

Compal Confidential

C5V08/C5V09/D5PR8 Schematics Document

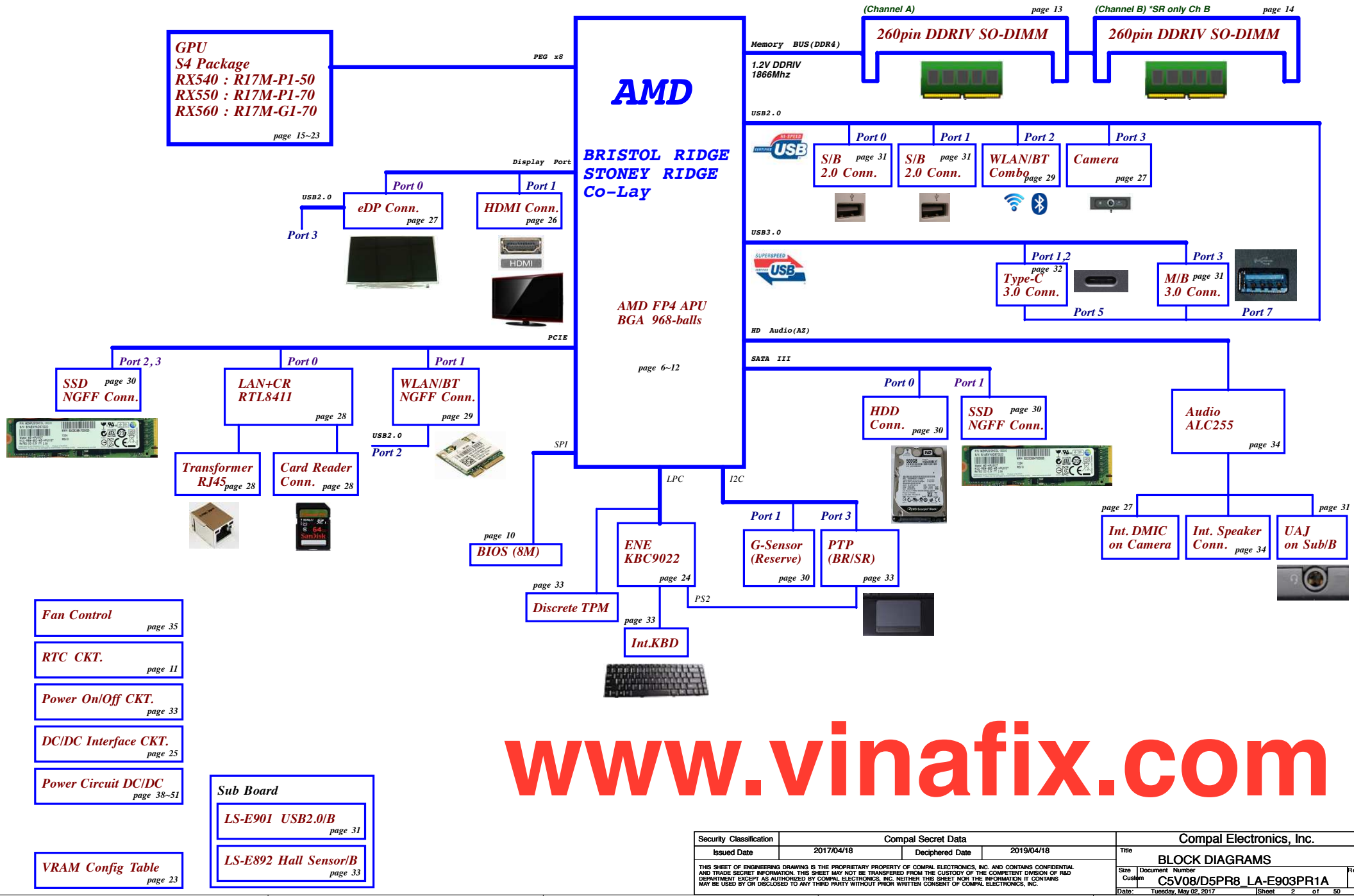
AMD Bristol Ridge/Stoney Ridge Platform

APU 15W/35W + Radeon R17M-P1-50/70/G1-70 25W/40W/50W

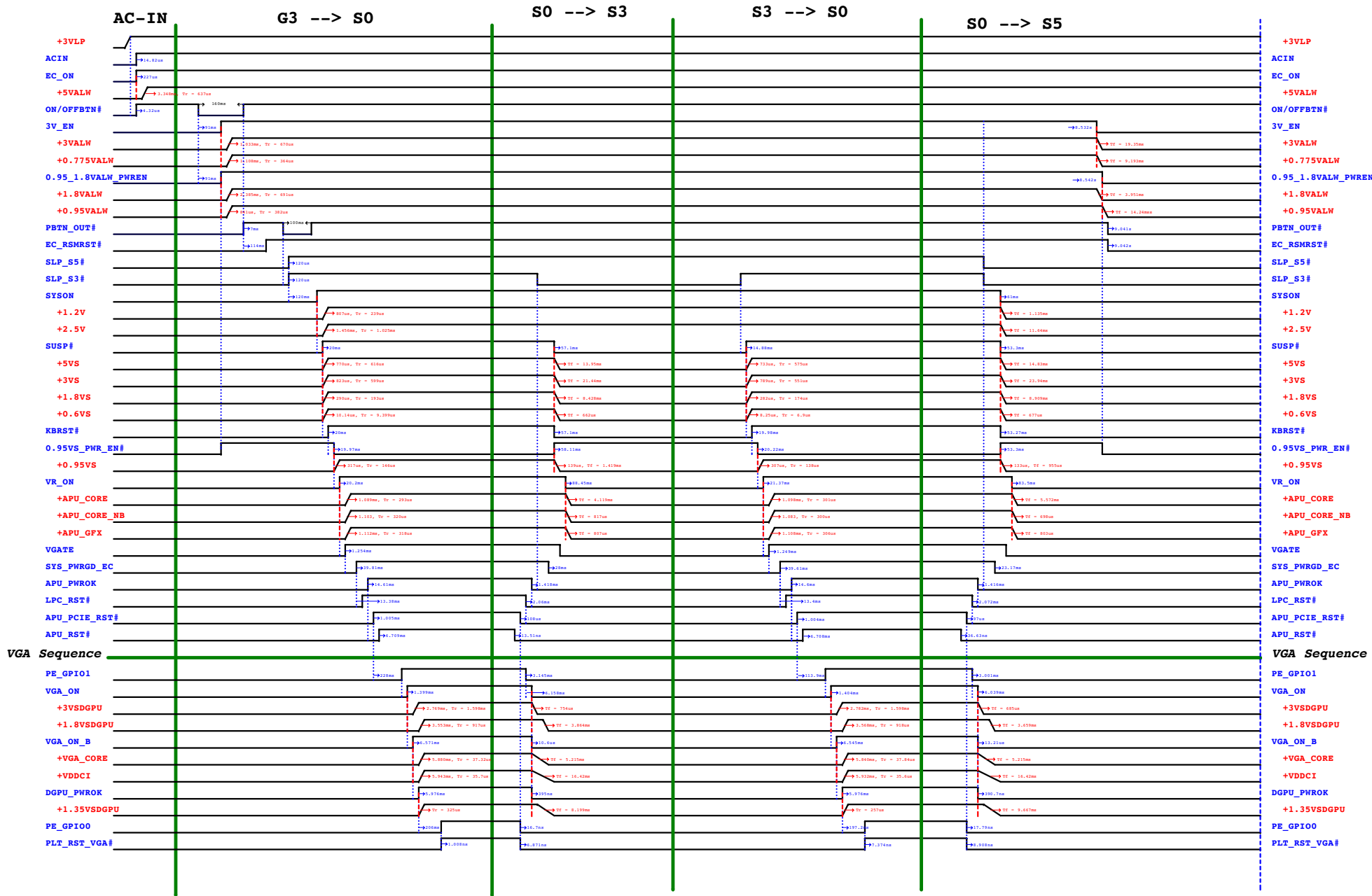
LA-E903P REV:1.A

2017-04-18

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				COVER PAGE	
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Voltage Rails

Power Plane	Description	S0	S3	S5
+19V_VIN	Adapter power supply (19V)	ON	ON	ON
+19VB	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+APU_CORE_GFX	Voltage for GFX	ON	OFF	OFF
+APU_CORE_FCH	Fusion Controller Hub Power Supply	ON	ON	ON
+0.95VALW	0.95V always on power rail	ON	ON	OFF
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail for APU and DDR	ON	ON	OFF
+1.2V	1.2V power rail for APU and DDR	ON	ON	OFF
+0.6VS	0.6V switched power rail for DDR terminator	ON	OFF	OFF
+0.775VALW	0.775V always on power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	AC-ON DC-OFF
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON
+3VSDGPU	VGA power	ON	OFF	OFF
+1.8VSDGPU	VGA power	ON	OFF	OFF
+VDDCI	VGA power	ON	OFF	OFF
+VGA_CORE	VGA power	ON	OFF	OFF

APU SMBus/I2C Address Table

Master	Device	Address[7:1]	Address [7:0]	
			Write	Read
I2C Port 0 (+1.8VS)				
I2C Port 1 (+1.8VS)	G-Sensor (Reserver)	0001 1000b 18h	0011 0000b 30h	0011 0001b 31h
I2C Port 2 (+3VS)				
SBMUS Port 0 (+3VS)	JDIMM1	0101 0000b 50h	1010 0000b A0h	1010 0001b A1h
	JDIMM2	0101 0001b 51h	1010 0010b A2h	1010 0011b A3h
I2C Port 3 (+3VALW)	PTP (Synaptics)	0010 1100b 2Ch	0101 1000b 58h	0101 1001b 59h
	PTP (ELAN)	0001 1111b 15h	0011 1110b 3Eh	0011 1111b 3Fh
SMBus Port 1 (+3VALW)				

EC SMBus Address Table

SMBus Address Table				
SMBus Port 1 (+3VALW)	Smart Battery	0000 1011b 0Bh	0001 0110b 16h	0001 0111b 17h
	Charger IC (BQ24735)	0000 1001b 09h	0001 0010b 12h	0001 0011b 13h
SMBus Port 2 (+3VS)	APU Temp. (TS1)	0100 1100b 4Ch	1001 1000b 98h	1001 1001b 99h
	GPU Temp.	0100 0001b 41h	1000 0010b 82h	1000 0011b 83h

BOARD ID Table

Board ID	PCB Revision
0	C5V08 EVT
1	C5V08 DVT
2	C5V08 PVT
3	C5V08 MP
4	D5PR8 DVT
5	D5PR8 PVT
6	D5PR8 MP
7	D5PR8_PVT_32P
8	D5PR8_MP_32P



PCB
DA8001C0010
PCB 218 LA-E903P REV1 MB 2

PCB
DAZ21800201
PCB C5V08 LA-E903P LS-E901P/E892P

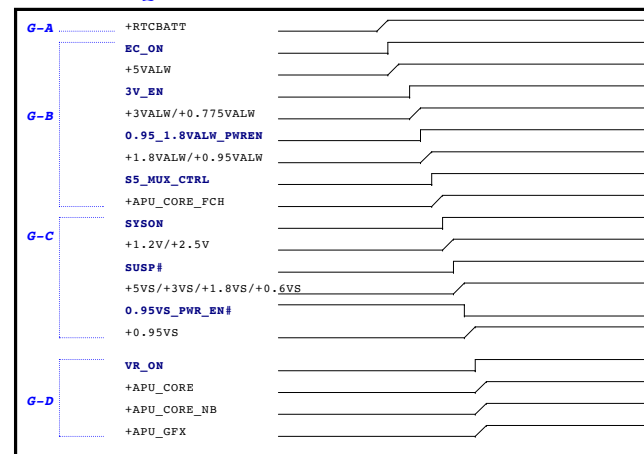
BOM Structure Table

BOM Structure	BTO Item
@	Unpop
@EMC@	EMI/ESD Unpop
EMC@	EMI/ESD pop
45@	HDMI Royalty
CONN@	ME Connector
JP@	Jump
RS@	R-Short
TP@	Test Point
TPM@	TPM Pop
PCIE@	PCIE SSD Device
SATA@	SATA SSD Device
T1@	Bristol Pop
T3@	Stoney Pop
GS@	G-Sensor Circuits
LDO@	RTL8411 LDO mode
SWR@	RTL8411 Switching mode
2D@	For 2 SO-DIMM use
PAR@	SATA Redriver PARADE solution
TI@	SATA Redriver TI solution
EVT@	Only use on EVT
CHG@	USB Charger
NCHG@	Non-USB Charger
UMA@	UMA Config
	CPU PN Refer p.6
EA@	EA Series
VX@	VX Series
DIS@	VGA Circuits Pop
V2G_s@	VRAM use SAMSUNG
V2G_h@	VRAM use HYNIX
V2G_m@	VRAM use MICRON
	GPU PN Refer p.23
RX540@	R17M-P1-50 GPU
RX550@	R17M-P1-70 GPU
RX560@	R17M-G1-70 GPU

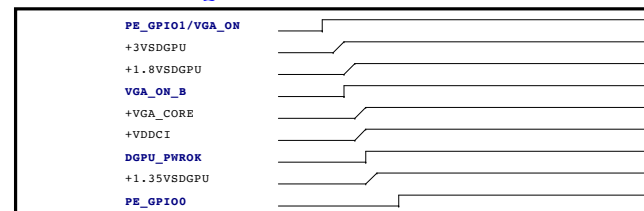
Board ID / SKU ID Table for AD channel

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xEF
19	NC	3.000V	3.300V		0xE7 - 0xFF

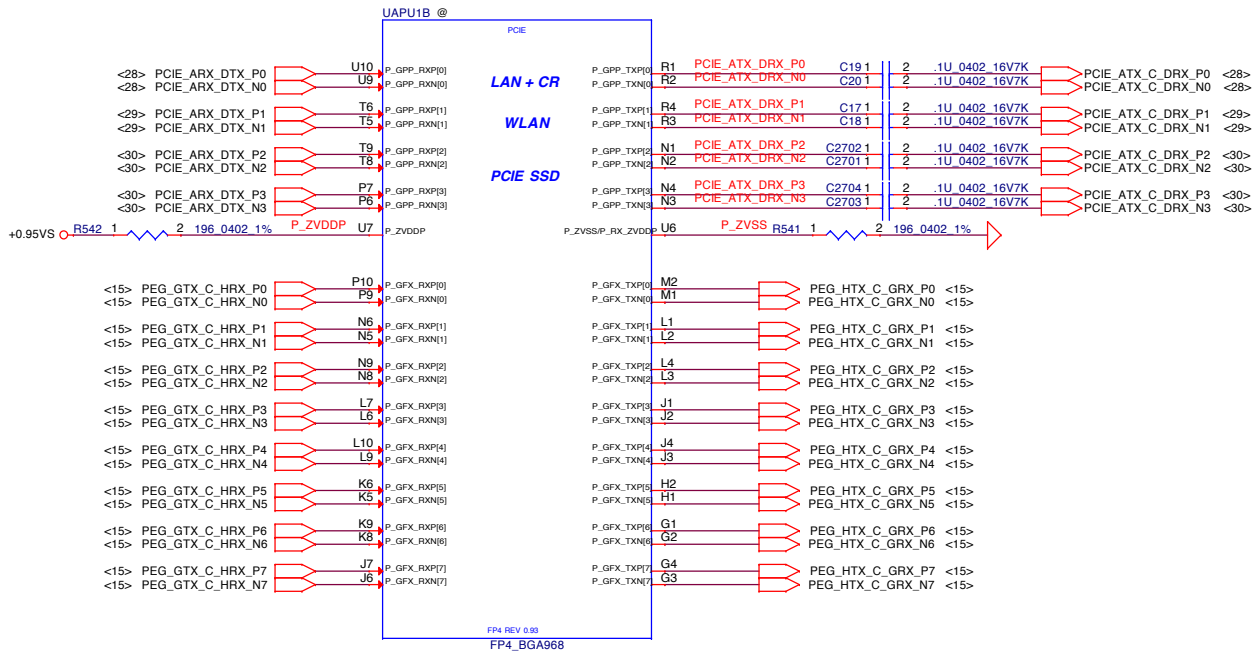
POWER SEQUENCE



VGA POWER SEQUENCE



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CPU PN Table

CPU Platform	PN R1(ROH)	PN R3(ABO!)
Bristol 15W	UAPU1 BR_A10@ S IC A10-9620P AM962PADY44AB 2.5G BGA 968P AP SA0000AK010	UAPU1 BR_A10R3@ S IC A10-9620P AM962PADY44AB 2.5G ABO! SA0000AK020
	UAPU1 BR_A12@ S IC A12-9720P AM972PADY44AB 2.7G BGA 968P AP SA0000AJY10	UAPU1 BR_A12R3@ S IC A12-9720P AM972PADY44AB 2.7G ABO! SA0000AJY20
	UAPU1 BR_FX@ S IC FX-9800P FM980PADY44AB 2.7G BGA 968P AP SA00009LB00	UAPU1 BR_FXR3@ S IC FX-9800P FM980PADY44AB 2.7G ABO! SA00009LB40

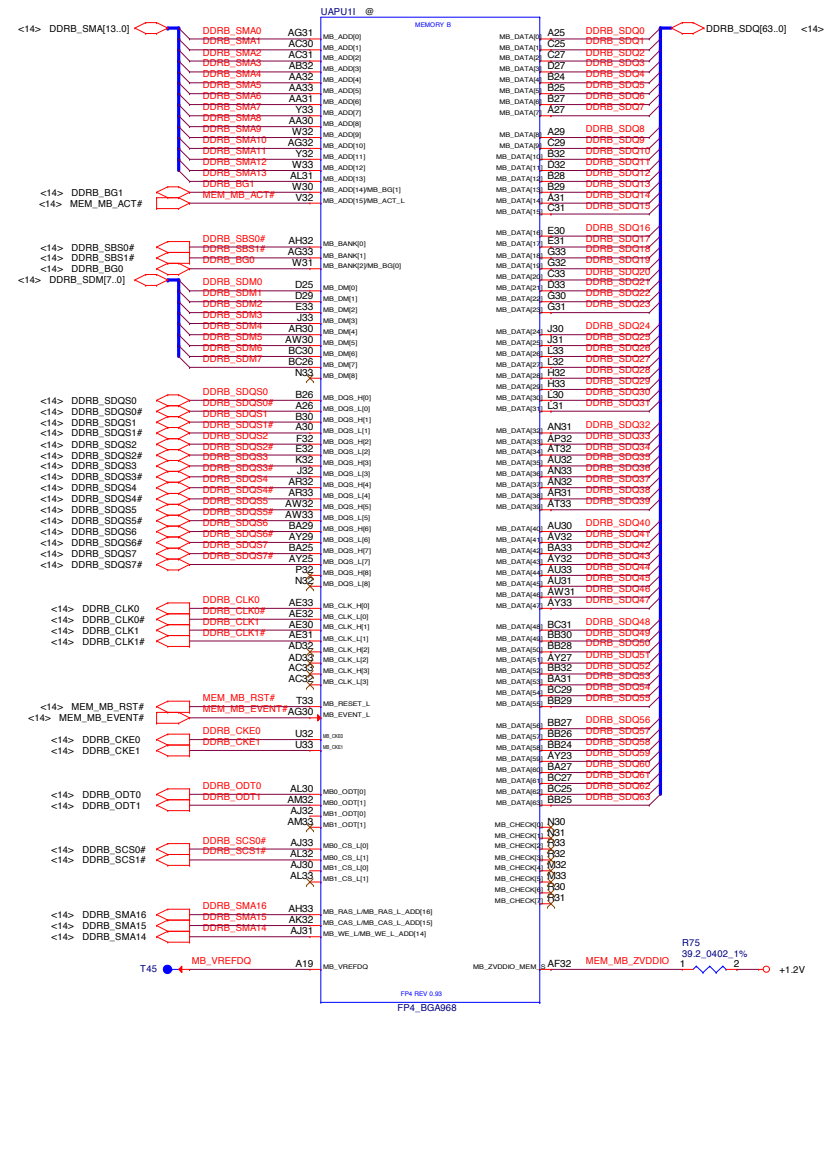
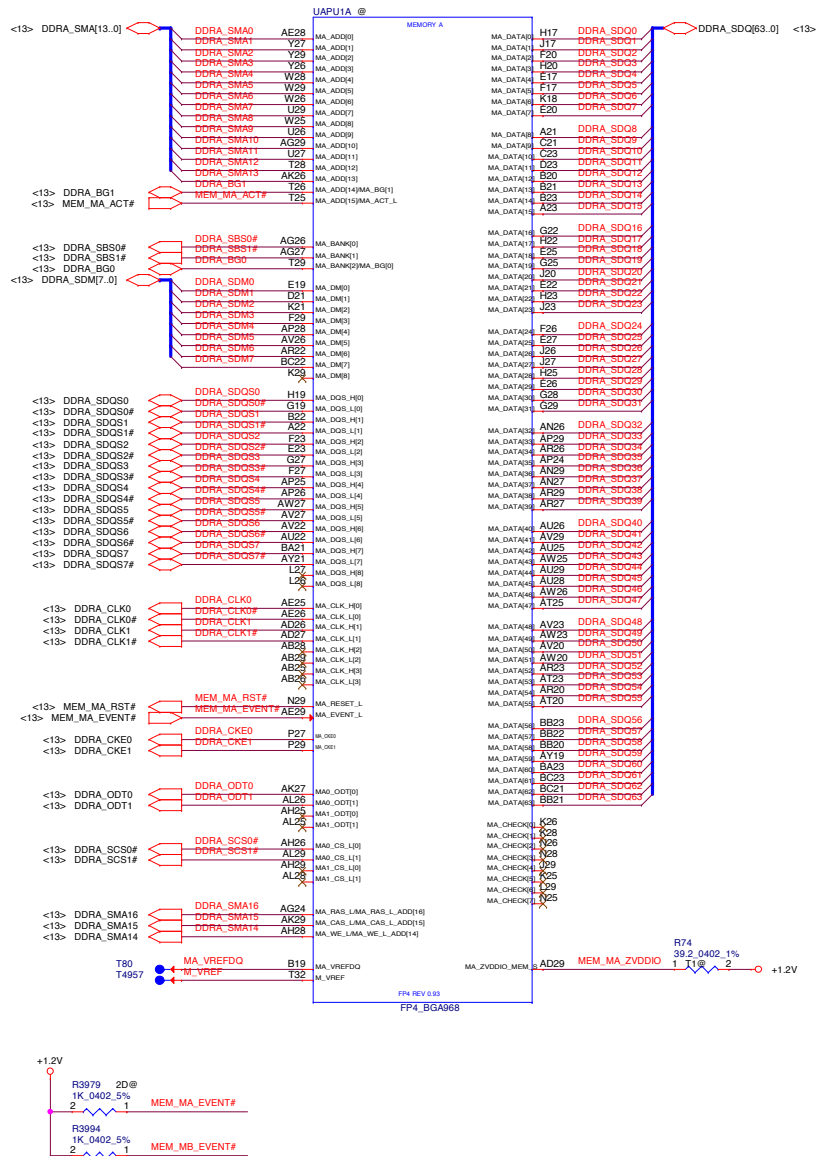
CPU PN Table

CPU Platform	PN R1(ROH)	PN R3(ABO!)
Bristol 35W	UAPU1 BR_35WA10@ S IC A10-9630P AM963PAEY44AB 2.6G BGA968 SA0000AOQ00	
	UAPU1 BR_35WA12@ S IC A12-9730P AM973PAEY44AB 2.8G BGA968 SA0000AOR00	
	UAPU1 BR_35WFX@ S IC FX-9830P FM983PAEY44AB 3G BGA 968P SA0000AOS00	

CPU PN Table

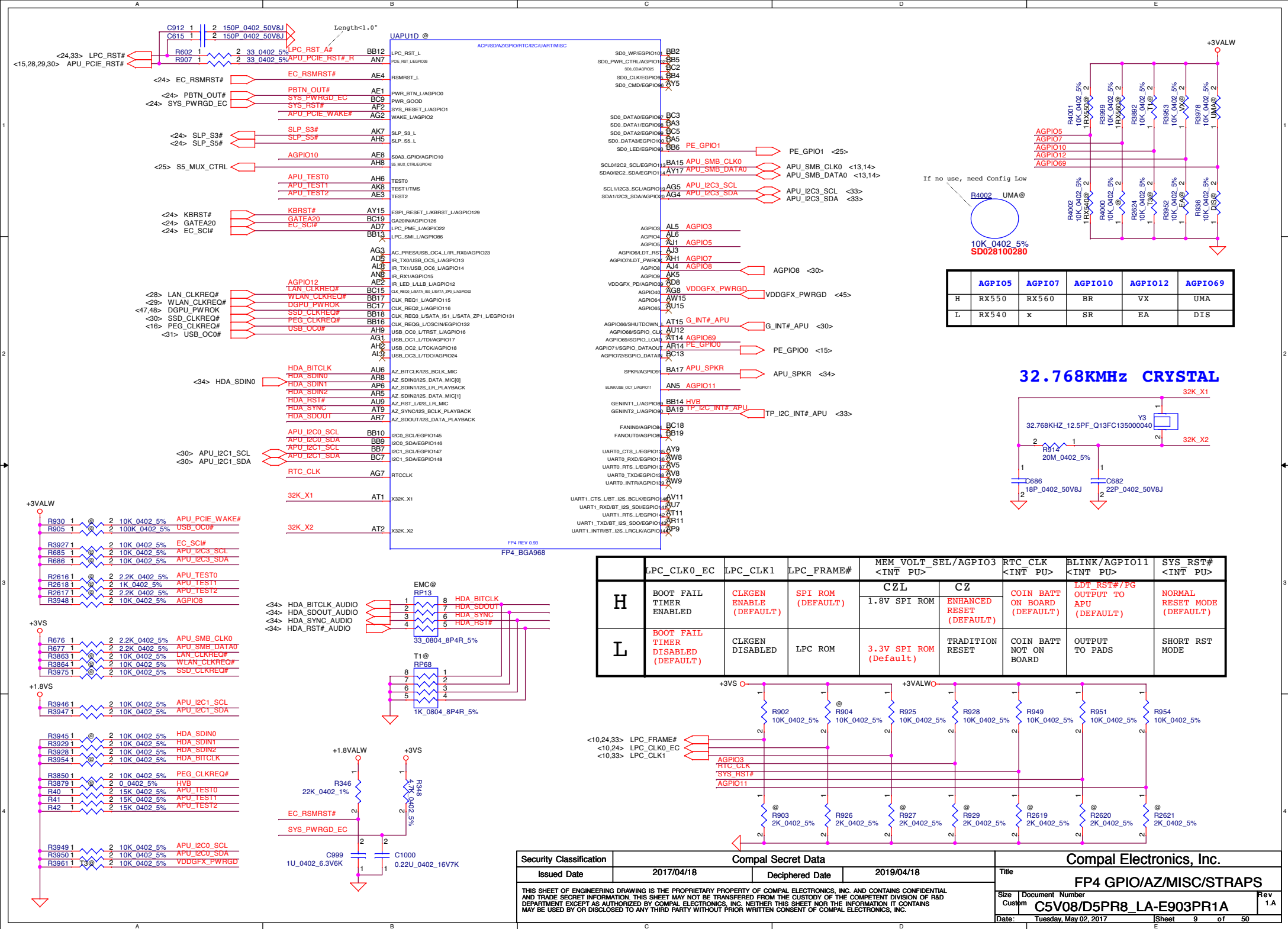
CPU Platform	PN R1(ROH)	PN R3(ABO!)
Stoney	UAPU1 SR_A6@ S IC A6-9220 AM9220AVY23AC 2.5G BGA 968P SA0000ALL00	UAPU1 SR_A6R3@ S IC A6-9220 AM9220AVY23AC 2.5G BGA ABO! SA0000ALL10

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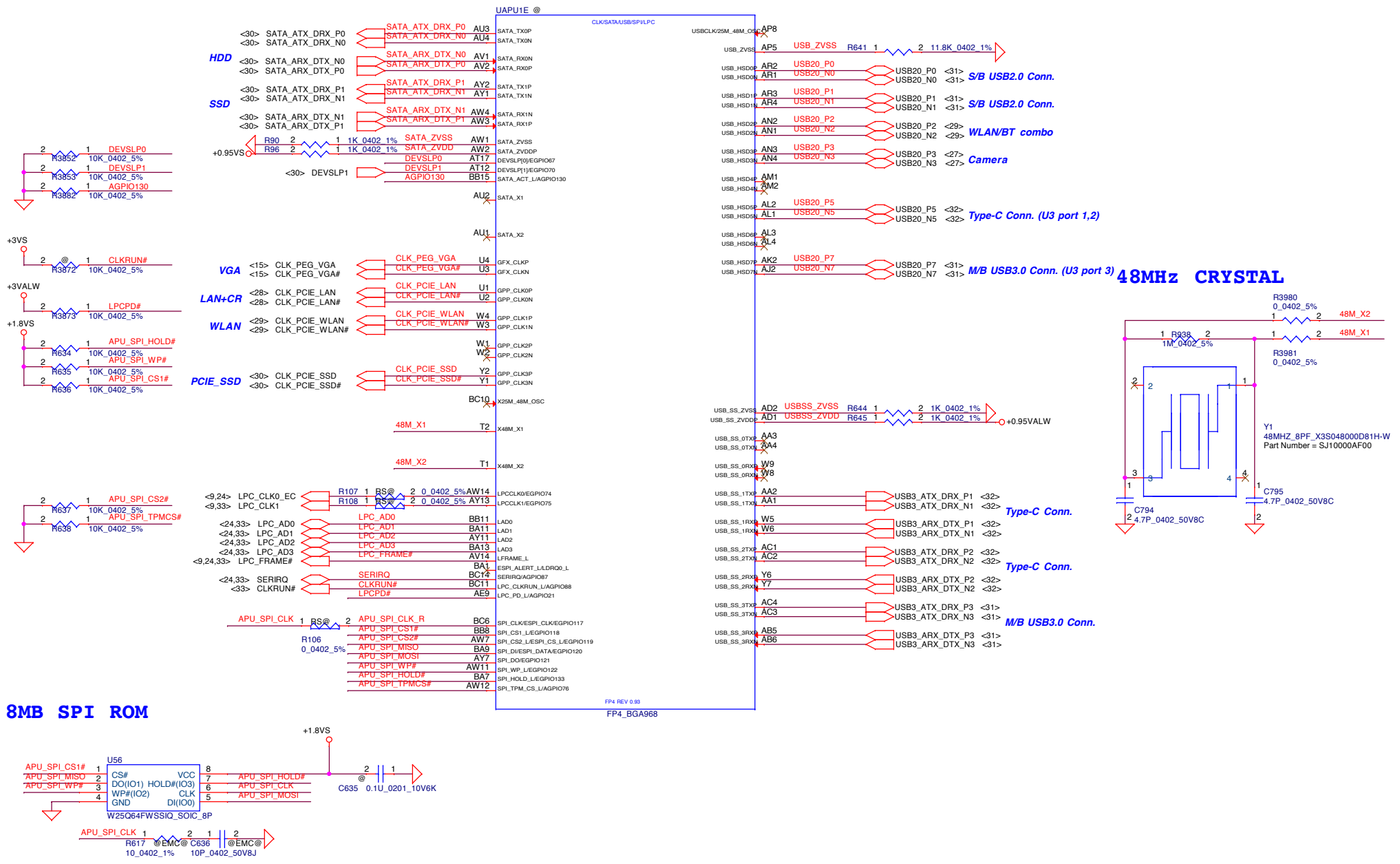


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	LPC_CLK0_EC	LPC_CLK1	LPC_FRAME#	MEM VOLT_SEL/AGPIO3 <INT PU>		RTC CLK <INT PU>	BLINK/AGPIO11 <INT PU>	SYS_RST# <INT PU>
H	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	SPI ROM (DEFAULT)	CZL	CZ	COIN BATT ON BOARD (DEFAULT)	LPT_RST#/PG OUTPUT TO APU (DEFAULT)	NORMAL RESET MODE (DEFAULT)
				1.8V SPI ROM	ENHANCED RESET (DEFAULT)			
L	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM (Default)	TRADITION RESET	COIN BATT NOT ON BOARD	OUTPUT TO PADS	SHORT RST MODE

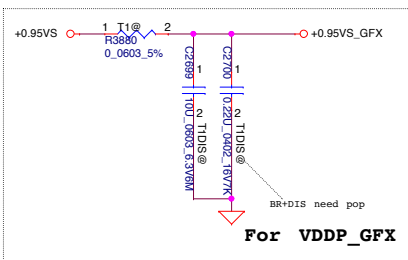
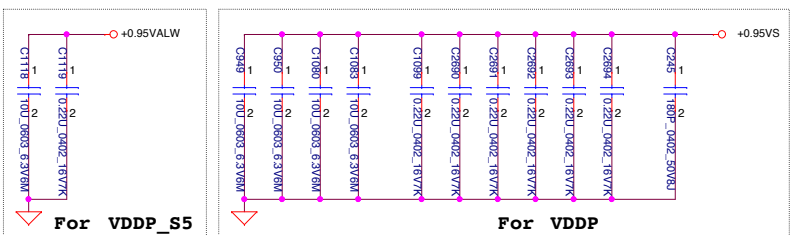
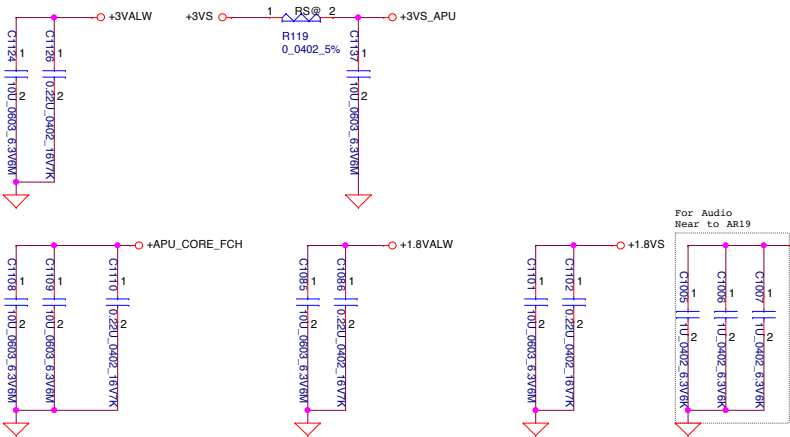
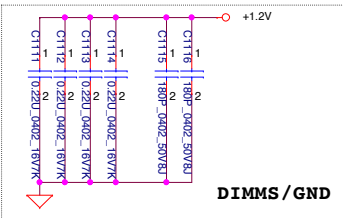
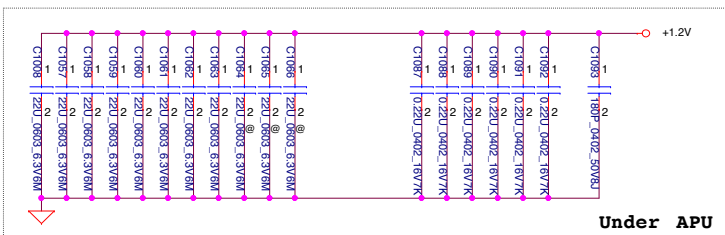
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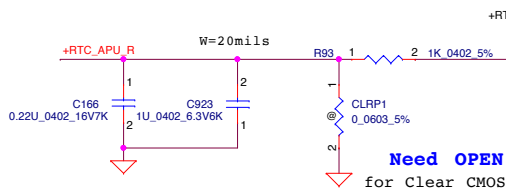
8MB SPI ROM

48MHz CRYSTAL

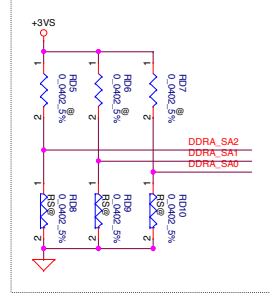
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								FP4 SATA/CLK/USB/SPI							
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RTC OF APU

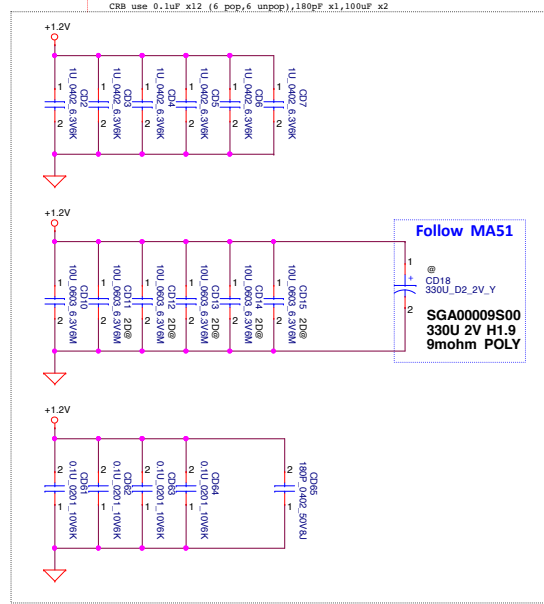


Address : A0



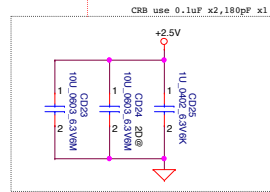
Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

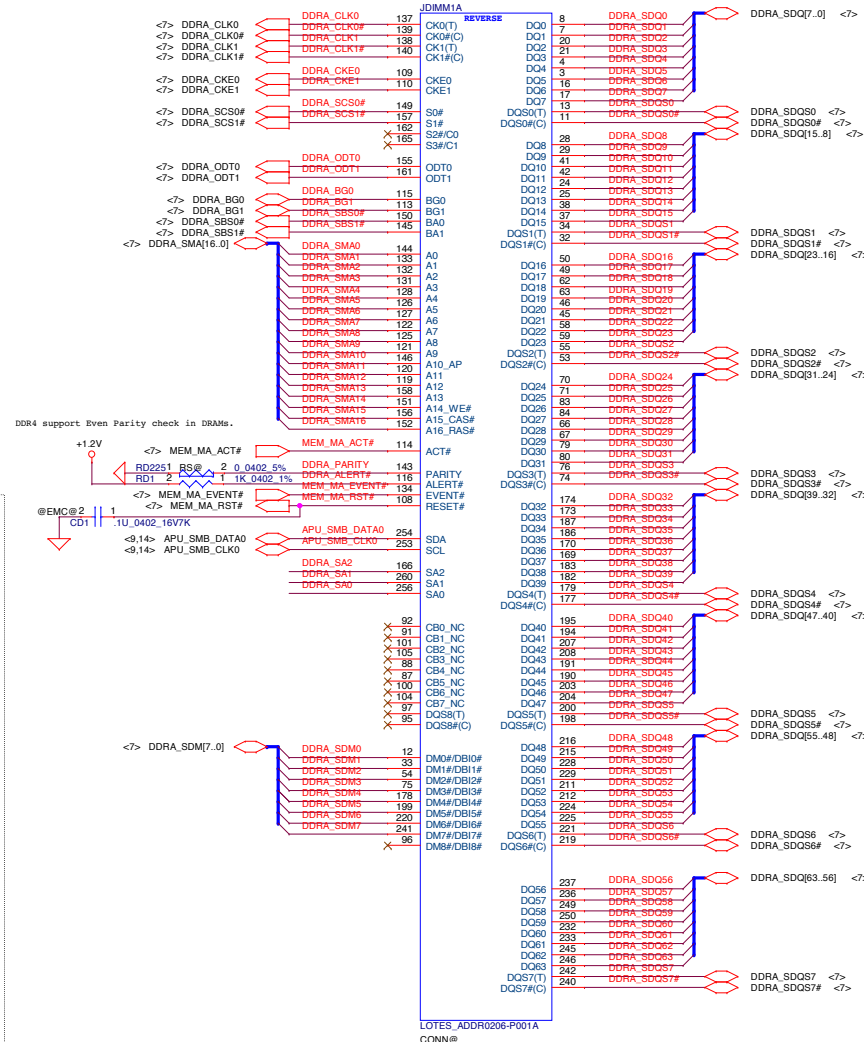
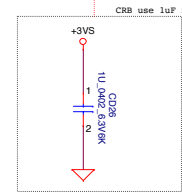


Follow MA51
SGA00009S00
330U 2V H1.9
9mohm POLY

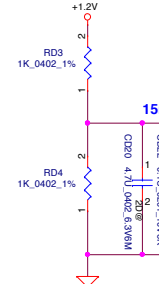
Layout Note:
Place near JDIMM1.257, 259



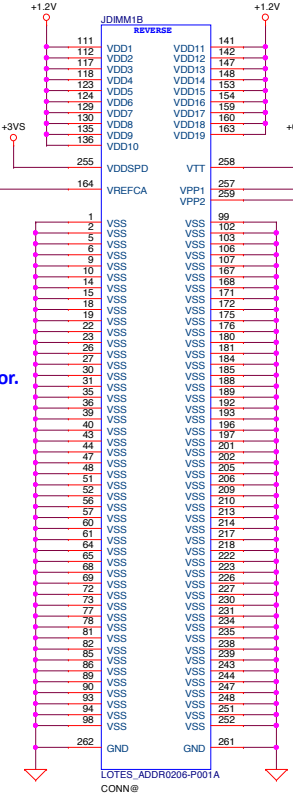
Layout Note:
Place near JDIMM1.255



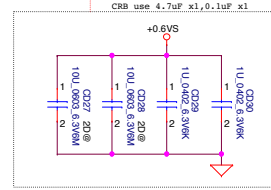
Follow CRB design



Place near to SO-DIMM connector.



Layout Note:
Place near JDIMM1.258



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Three circuit diagrams showing the connection of capacitors CDB6, CDB7, CDB8, CDB9, and CDB5 to a +1.2V supply and ground. Each diagram shows a capacitor connected in parallel between the +1.2V line and ground, with its value and tolerance specified.

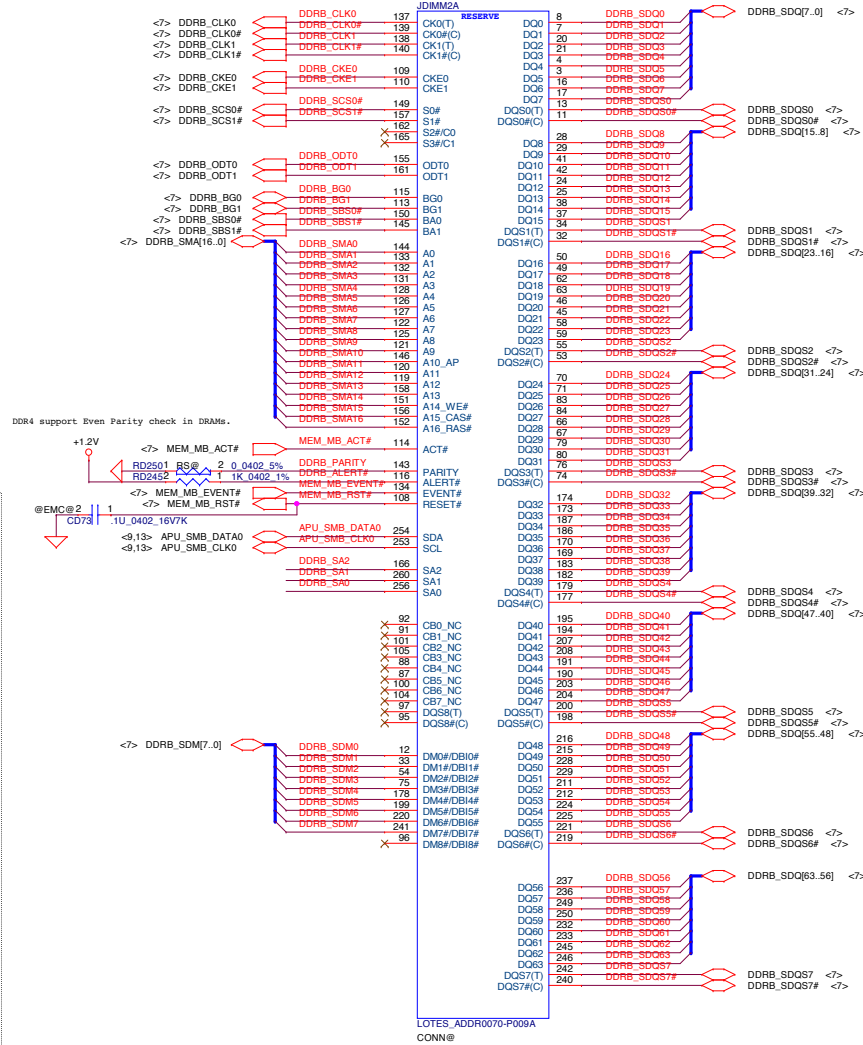
Diagram 1 (CDB6, CDB7, CDB8): Shows three capacitors connected in parallel between the +1.2V supply and ground. CDB6 is 10.0002 6.390K, CDB7 is 10.0002 6.390K, and CDB8 is 10.0002 6.390K.

Diagram 2 (CDB9): Shows a single capacitor connected in parallel between the +1.2V supply and ground. CDB9 is 100.0002 6.390M.

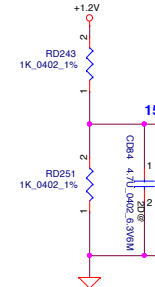
Diagram 3 (CDB5): Shows a single capacitor connected in parallel between the +1.2V supply and ground. CDB5 is 180P 0.002 50V/SJ.

CRB use 0.1uF x2, 180pF x1

The diagram shows a parallel circuit with three capacitors connected to a +2.5V supply and ground. The capacitors are labeled CD79, CD85, and CD75. Each capacitor has a value of 10u 0003 6.3V0M and is connected with pin 1 to the supply and pin 2 to ground.



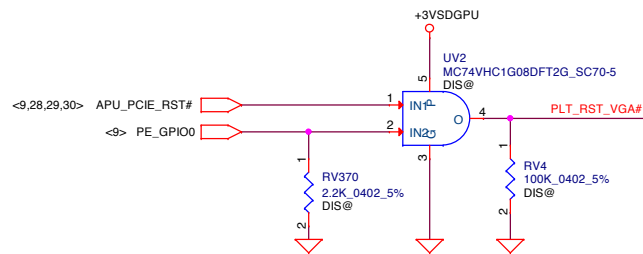
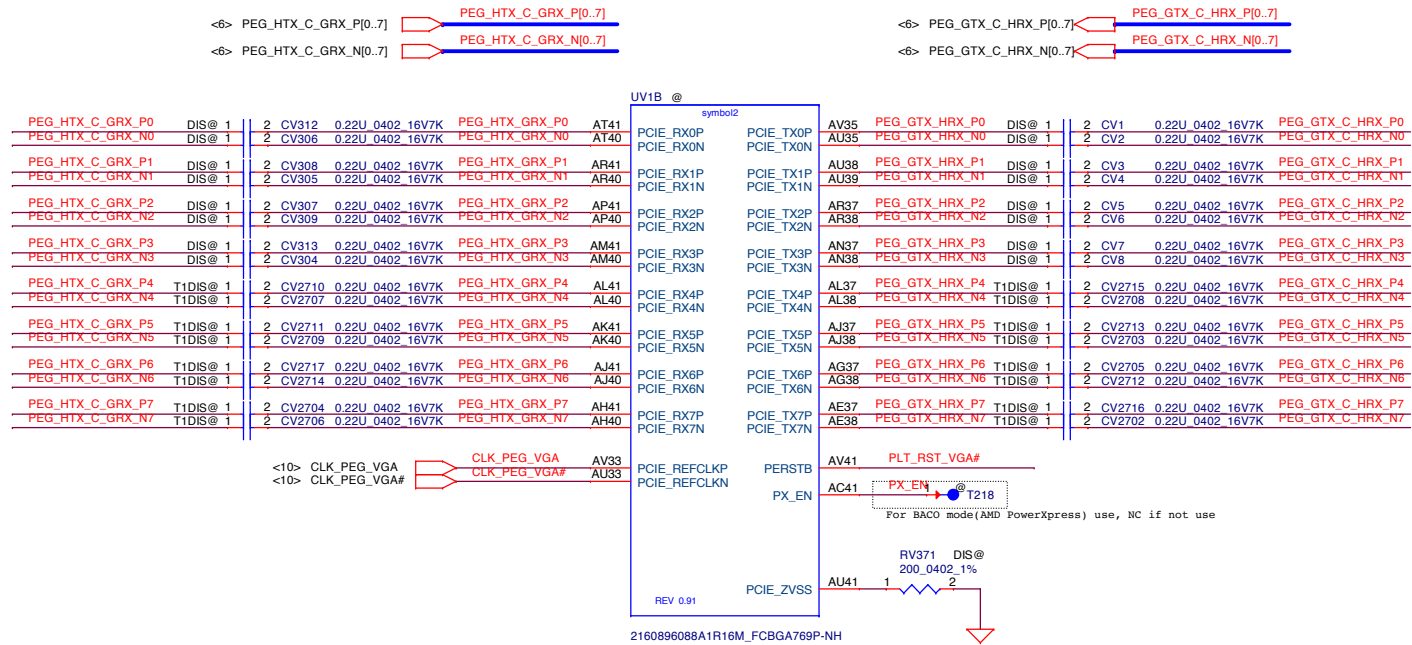
Follow CRB design

[illegible]

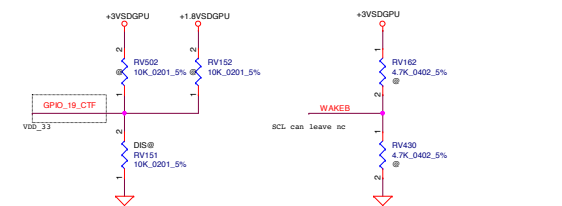
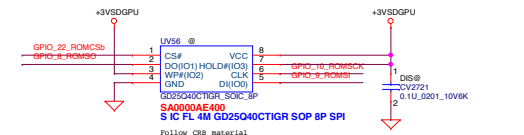
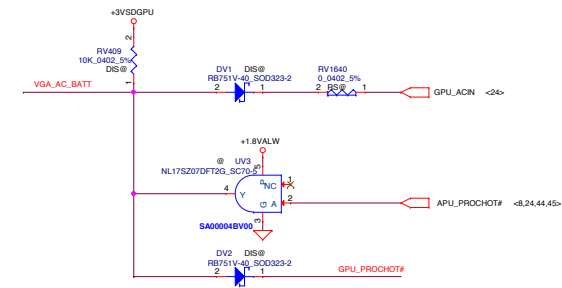
CRB use 4.7uF x1, 0.1uF x1

The diagram shows a circuit with four parallel branches connected to a +0.6V supply and ground. Each branch contains a 100,000 ohm resistor (CD70, CD74, CD32, CD72) in series with a 100,000 ohm resistor (100,000, 100,000, 100,000, 100,000).

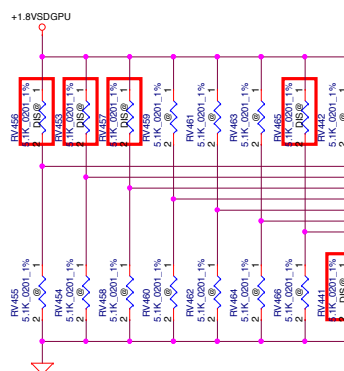
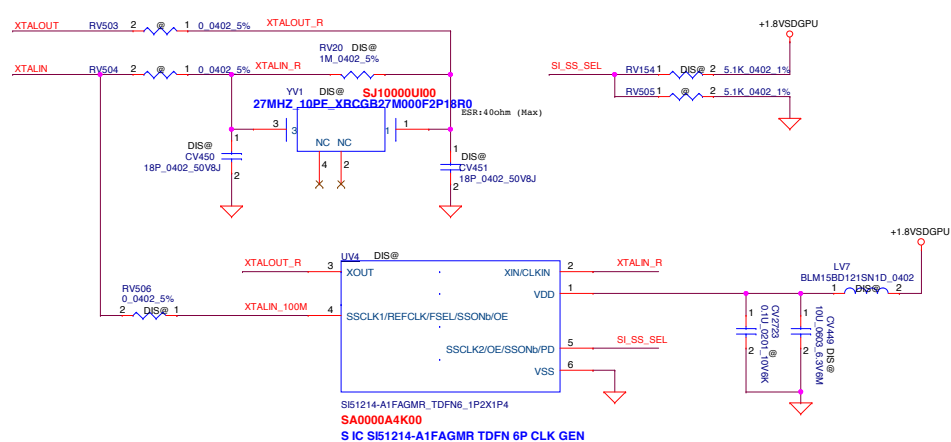
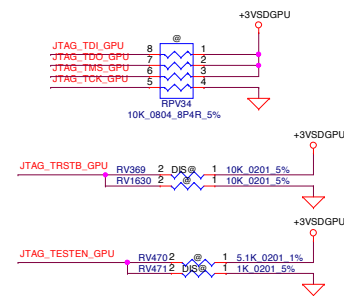
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				Custom	C5V08/D5PR8_LA-E903PR1A	1A
				Date:	Tuesday, May 02, 2017	Sheet



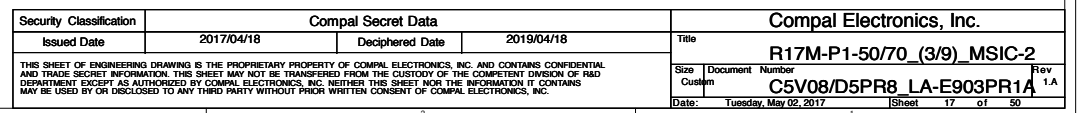
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/04/18	Deciphered Date	2019/04/18	Title	
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Size	Document	Number	Rev	C5V08/D5PR8_LA-E903PR1A	
Date:	Tuesday, May 02, 2017	Sheet	15	of	50

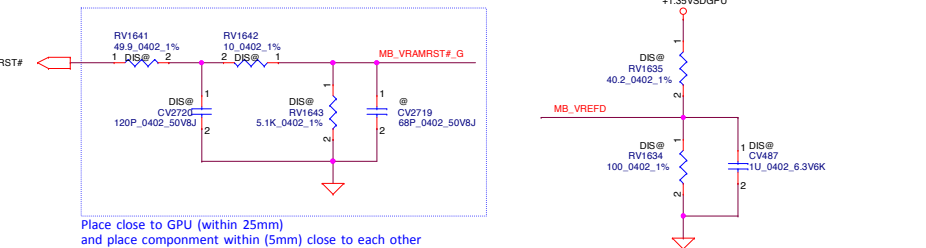
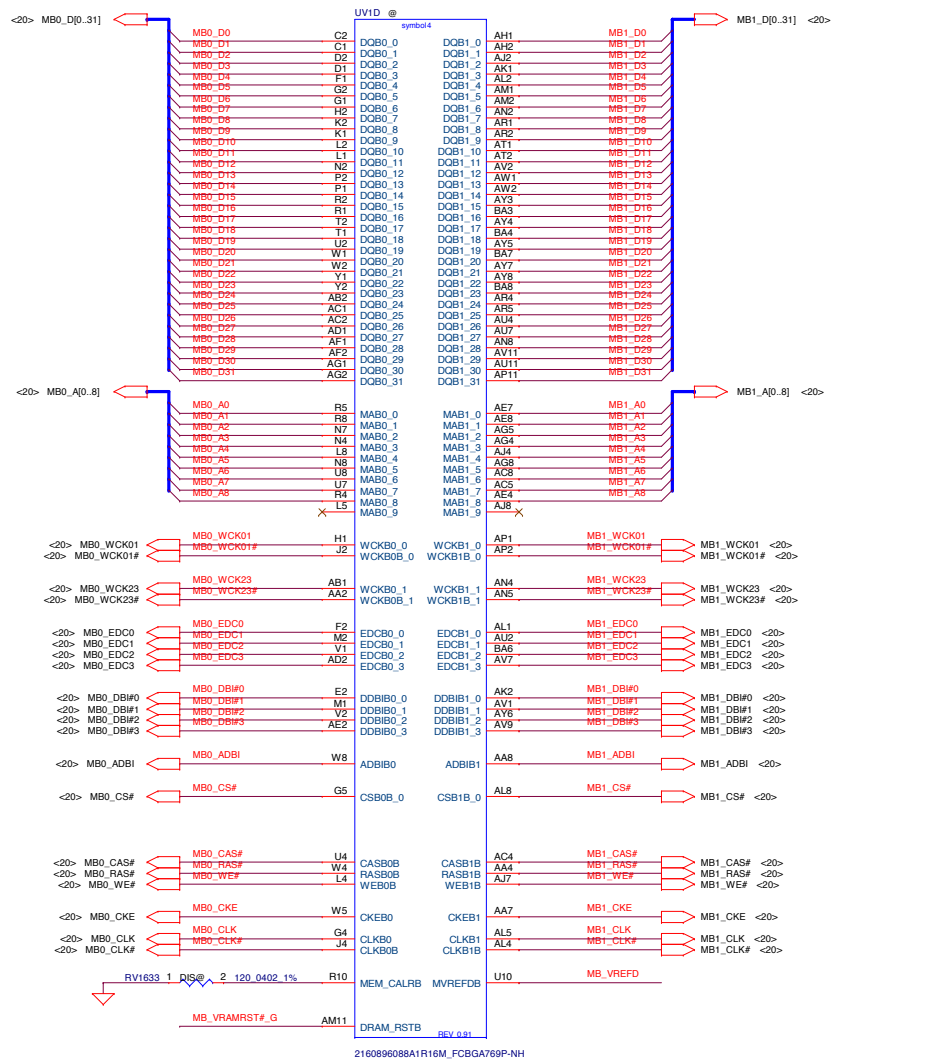
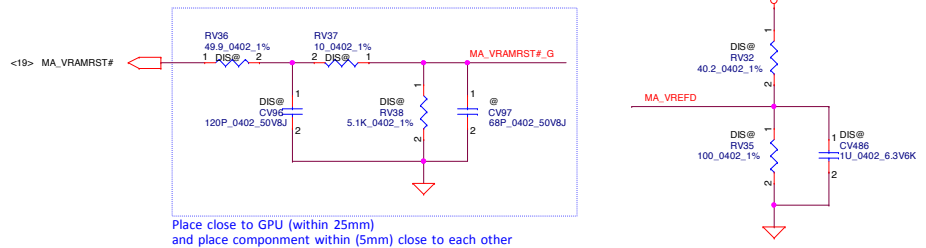
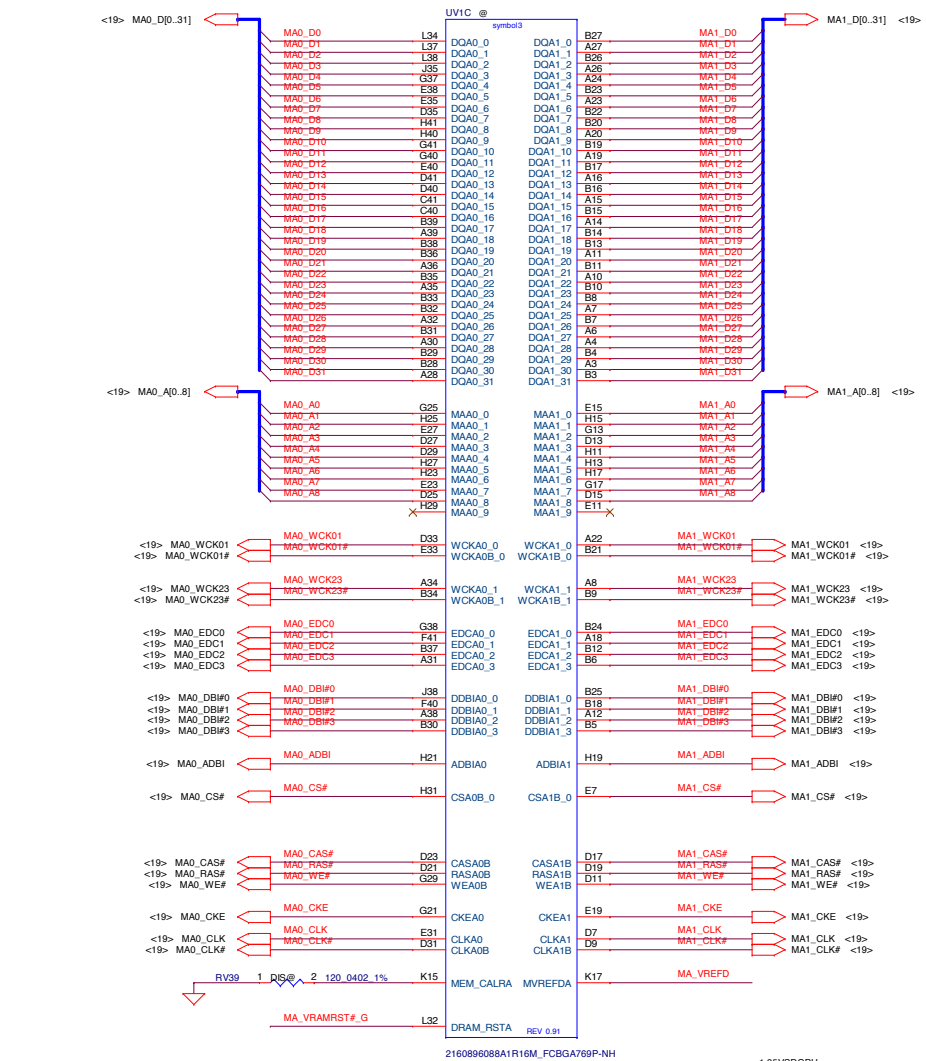


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				Date:	Tuesday, May 02, 2017		
					[Sheet 16 of 51]		

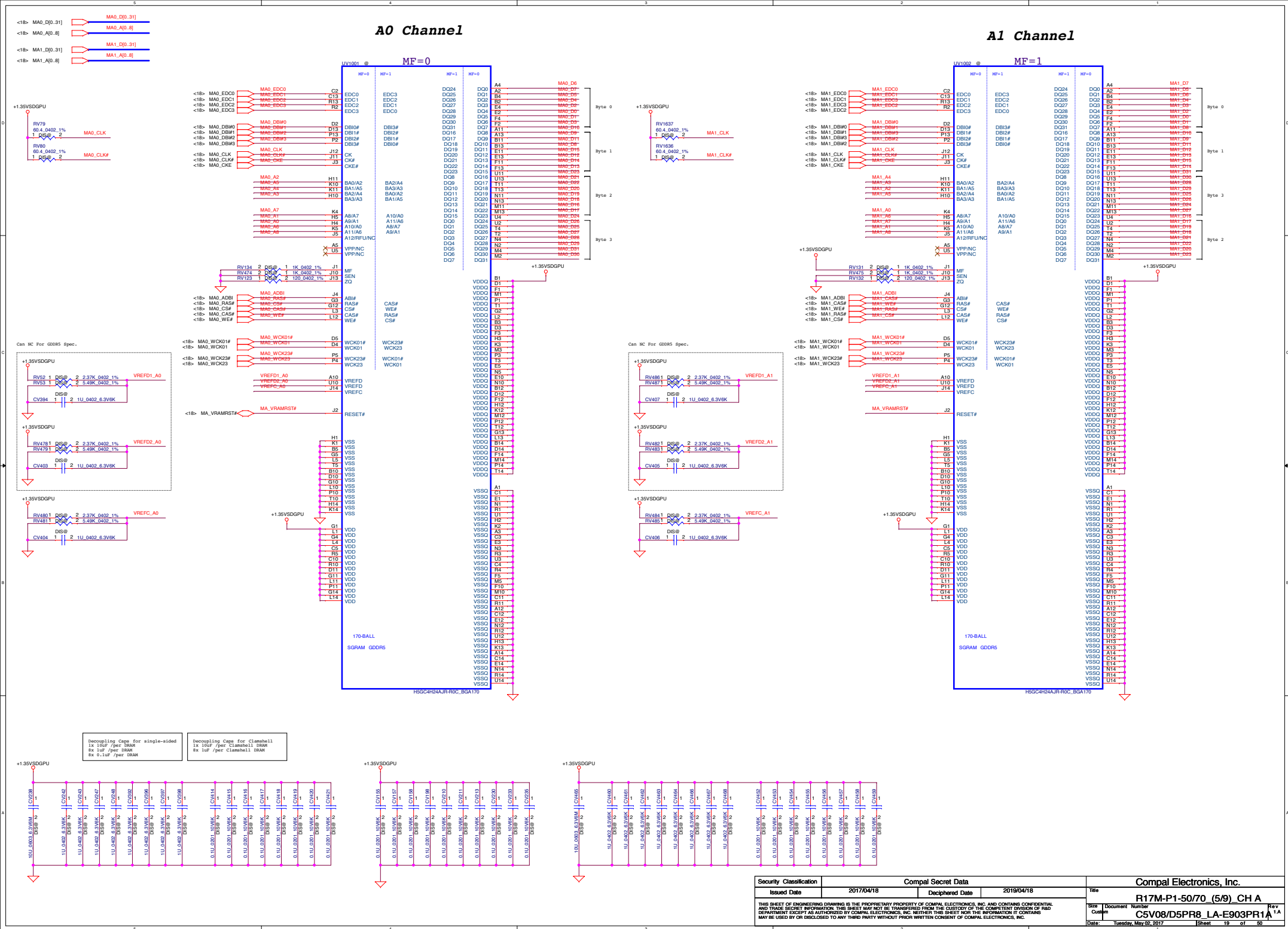


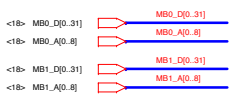
DBGDATA_[7:6]	
00:	0x 40
01:	0x 41
10:	0x 42
11:	0x 43





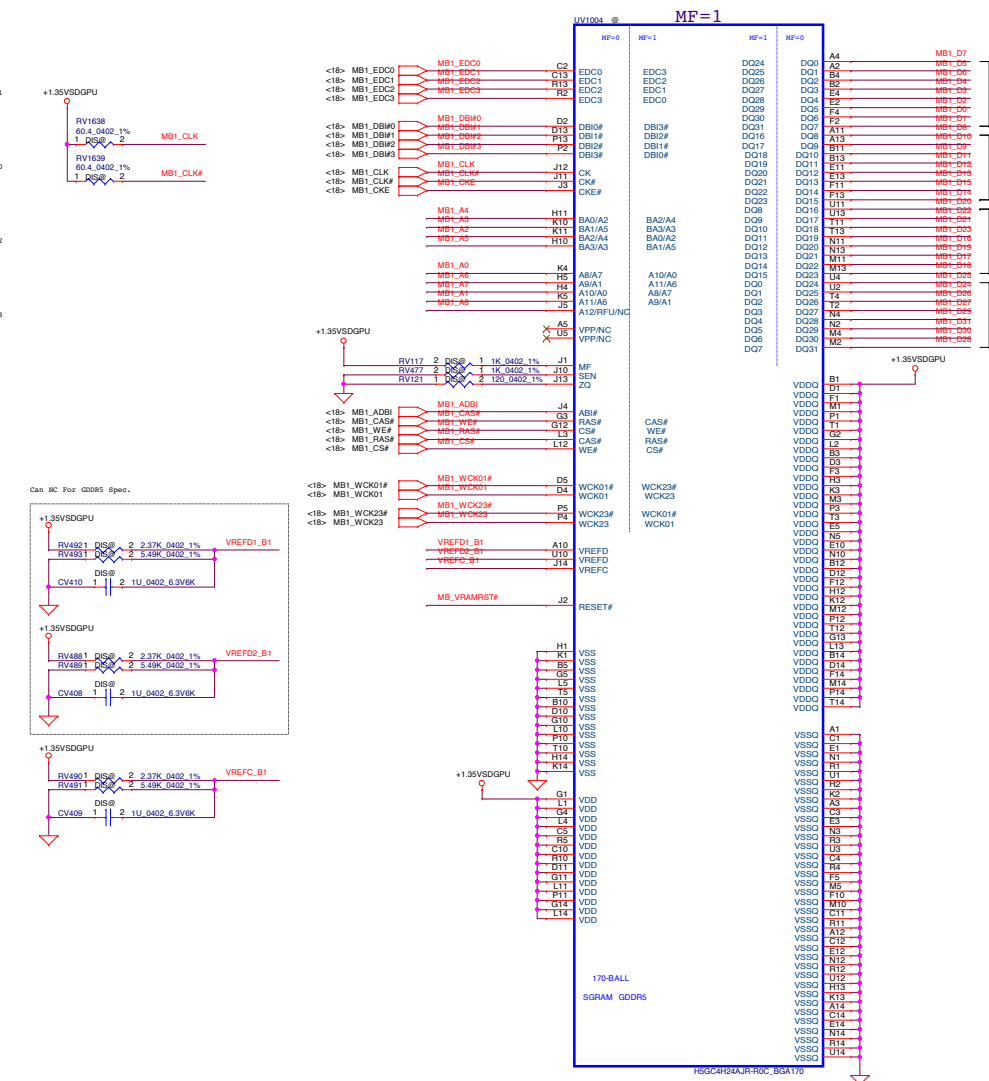
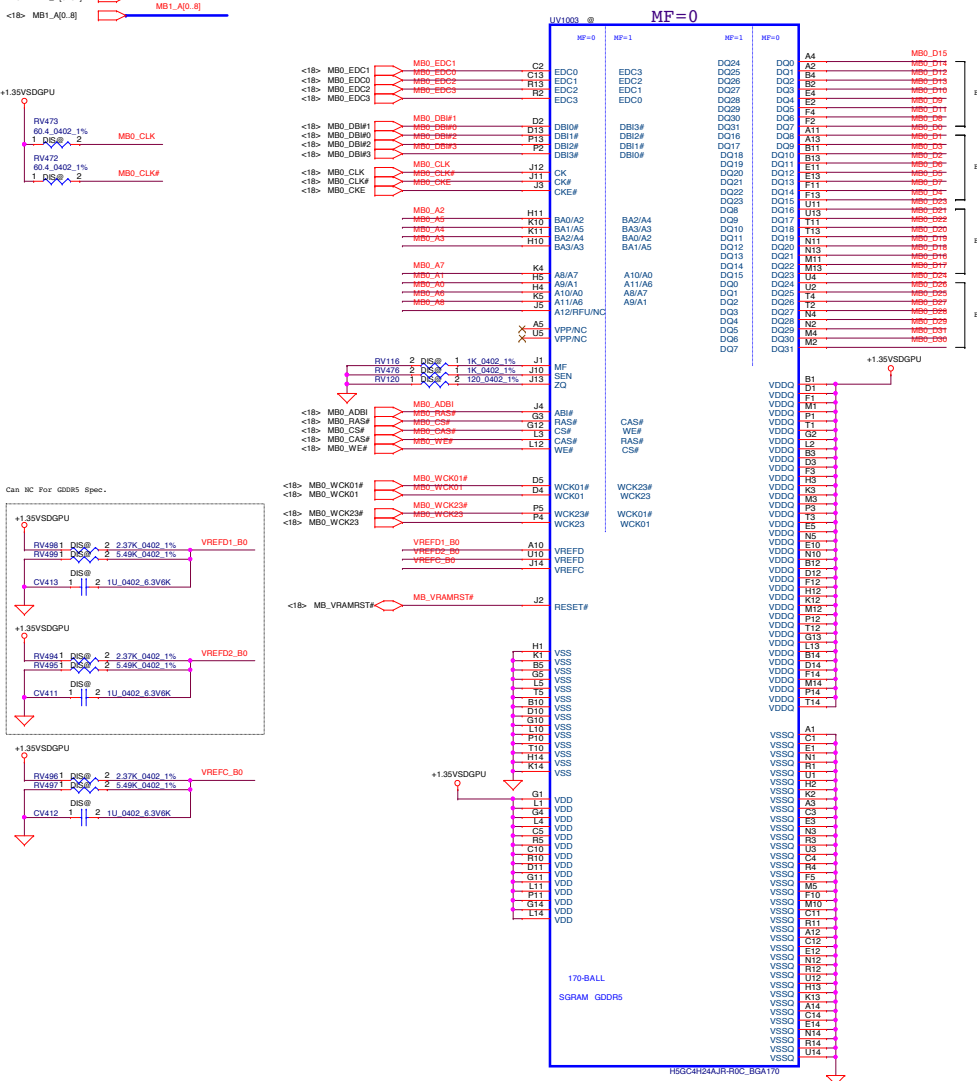
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				Date:	Tuesday, May 02, 2017
				Sheet	18 of 50





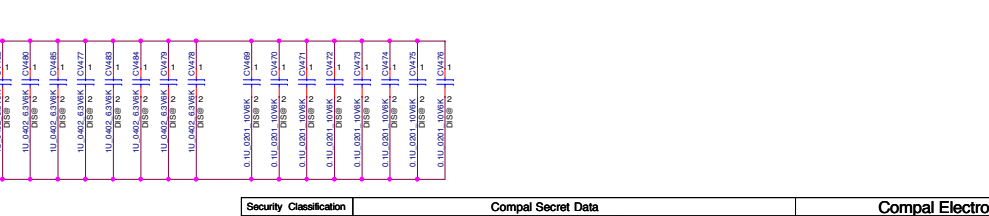
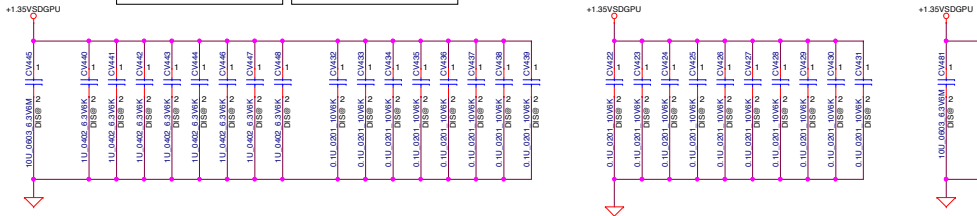
B0 Channel

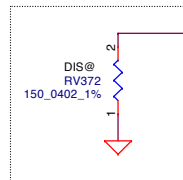
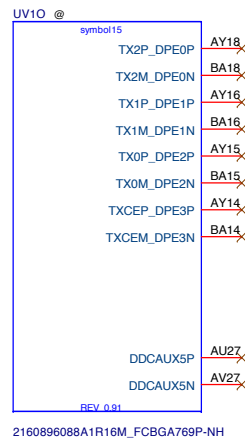
B1 Channel



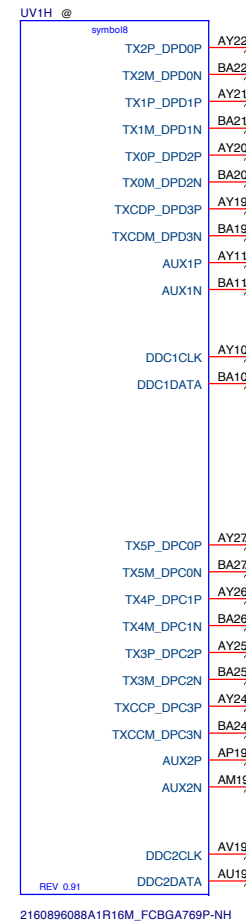
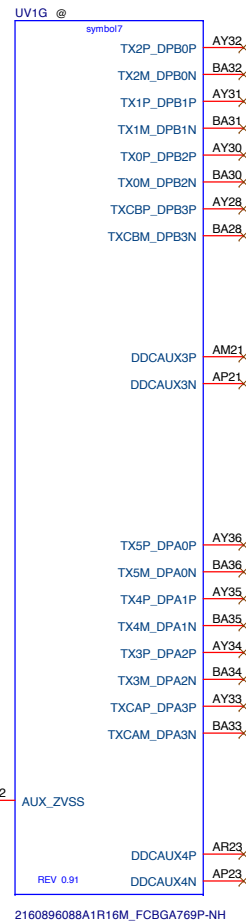
Decoupling Caps for single-sided
1x 10uF / per board
8x 1uF / per board
8x 0.1uF / per board

Decoupling Caps for Clamshell
1x 10uF / per Clamshell board
8x 1uF / per Clamshell board
8x 0.1uF / per Clamshell board





Data Book: need
config even if not
use display function

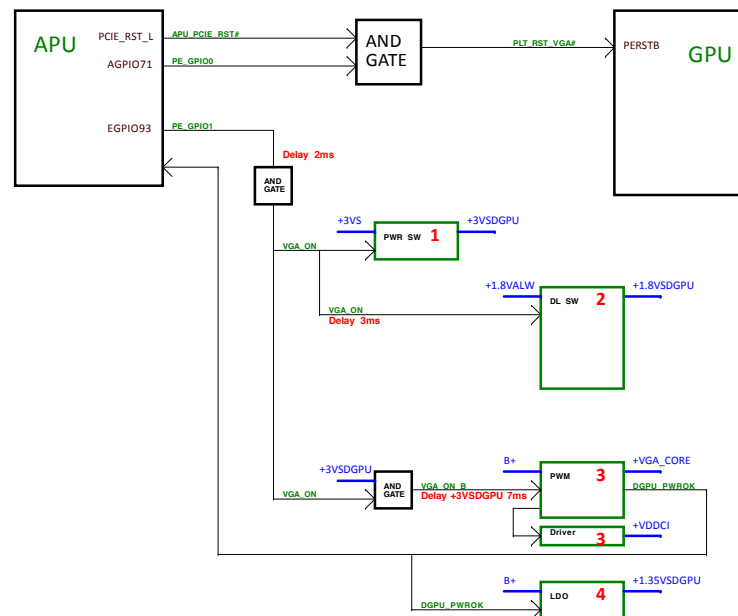
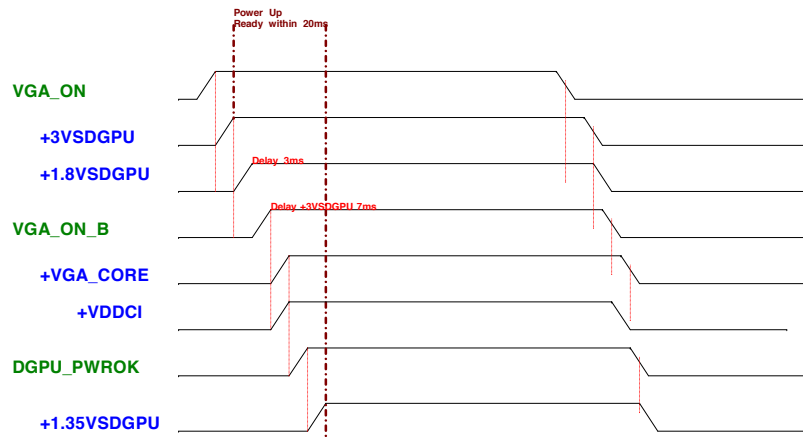


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				Custom	C5V08/D5PR8_LA-E903PR1A
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5.3 Power-up/down Sequence

"R17M-P1-50 / R17M-P1-70" has the following requirements with regards to power-supply sequencing to avoid damaging the GPU:




- All the GPU supplies, except for VDD_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 20 mV/ μ s.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10 μ s before VDDC, VDDCI, VDD_08, and VMEMIO start to ramp up.

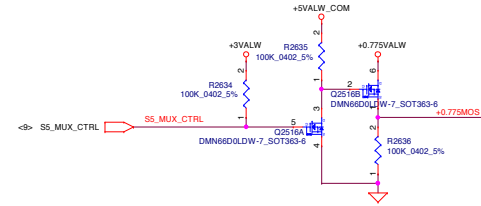
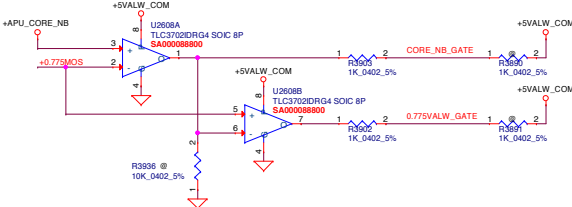
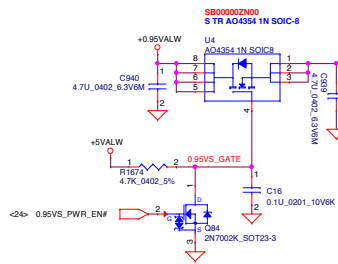
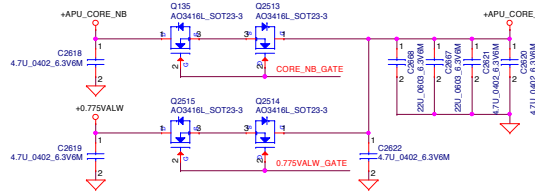
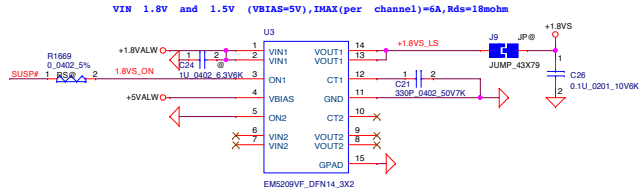
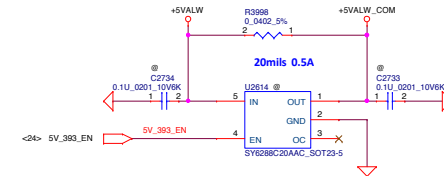
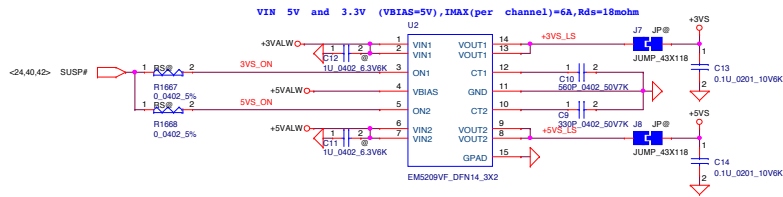


For AMD R17M-P1-50/70 VRAM Only

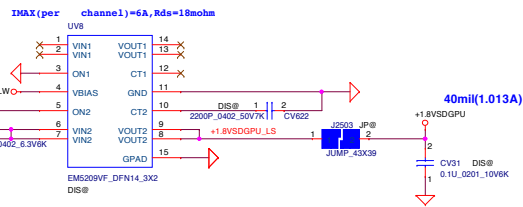
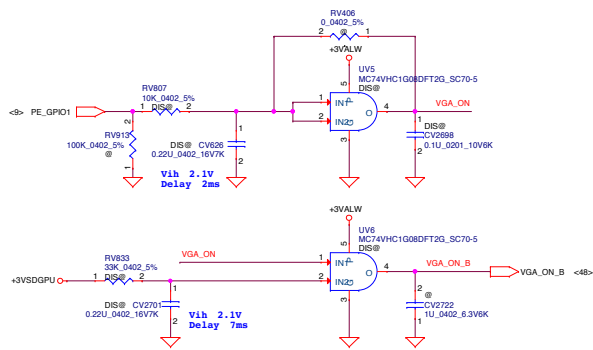
Memory ID/Vendor/Size	Memory PN R3(ABOI) A0	Memory PN R3(ABOI) A1	Memory PN R3(ABOI) B0	Memory PN R3(ABOI) B1
000 SAMSUNG 256M x32	 S IC D5 256M32 K4G80325FB-HC03 FBGA ABOI SA000094R30	 S IC D5 256M32 K4G80325FB-HC03 FBGA ABOI SA000094R30	 S IC D5 256M32 K4G80325FB-HC03 FBGA ABOI SA000094R30	 S IC D5 256M32 K4G80325FB-HC03 FBGA ABOI SA000094R30
001 HYNIX 256M x32	 S IC D5 256M32 H5GC8H24MJR-T2C BGA ABOI SA000092G20	 S IC D5 256M32 H5GC8H24MJR-T2C BGA ABOI SA000092G20	 S IC D5 256M32 H5GC8H24MJR-T2C BGA ABOI SA000092G20	 S IC D5 256M32 H5GC8H24MJR-T2C BGA ABOI SA000092G20
010 SAMSUNG 128M x32	 S IC D5 128M32 K4G41325FE-HC28 FBGA ABOI SA000091T30	 S IC D5 128M32 K4G41325FE-HC28 FBGA ABOI SA000091T30	 S IC D5 128M32 K4G41325FE-HC28 FBGA ABOI SA000091T30	 S IC D5 128M32 K4G41325FE-HC28 FBGA ABOI SA000091T30
011 HYNIX 128M x32	 S IC D5 128M322.5G H5GC4H24AJR-T2C ABOI SA000085V70	 S IC D5 128M322.5G H5GC4H24AJR-T2C ABOI SA000085V70	 S IC D5 128M322.5G H5GC4H24AJR-T2C ABOI SA000085V70	 S IC D5 128M322.5G H5GC4H24AJR-T2C ABOI SA000085V70
100 MICRON 256M x32	 S IC D5 256M32 MT51J256M32HF-60A ABOI SA000096K30	 S IC D5 256M32 MT51J256M32HF-60A ABOI SA000096K30	 S IC D5 256M32 MT51J256M32HF-60A ABOI SA000096K30	 S IC D5 256M32 MT51J256M32HF-60A ABOI SA000096K30

AMD GPU PN

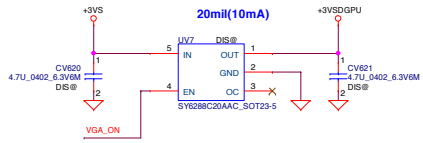
<p>R17M-P1-50 PN R1(ROH)</p> <p>UV1 RX540 @</p>  <p>S IC 216-0905018 A1 R17M-P1-50 FCBGA 769P 0FA SA0000ALV10</p>	
<p>R17M-P1-70 PN R1(ROH)</p> <p>UV1 RX550 @</p>  <p>S IC 216-0905004 A1 R17M-P1-70 FCBGA 769P 0FA SA0000ALX10</p>	
<p>R17M-G1-70 PN R1(ROH)</p> <p>UV1 RX560 @</p>  <p>S IC 216-0909004 A1 R17M-G1-70 FCBGA 0FA SA0000APU00</p>	



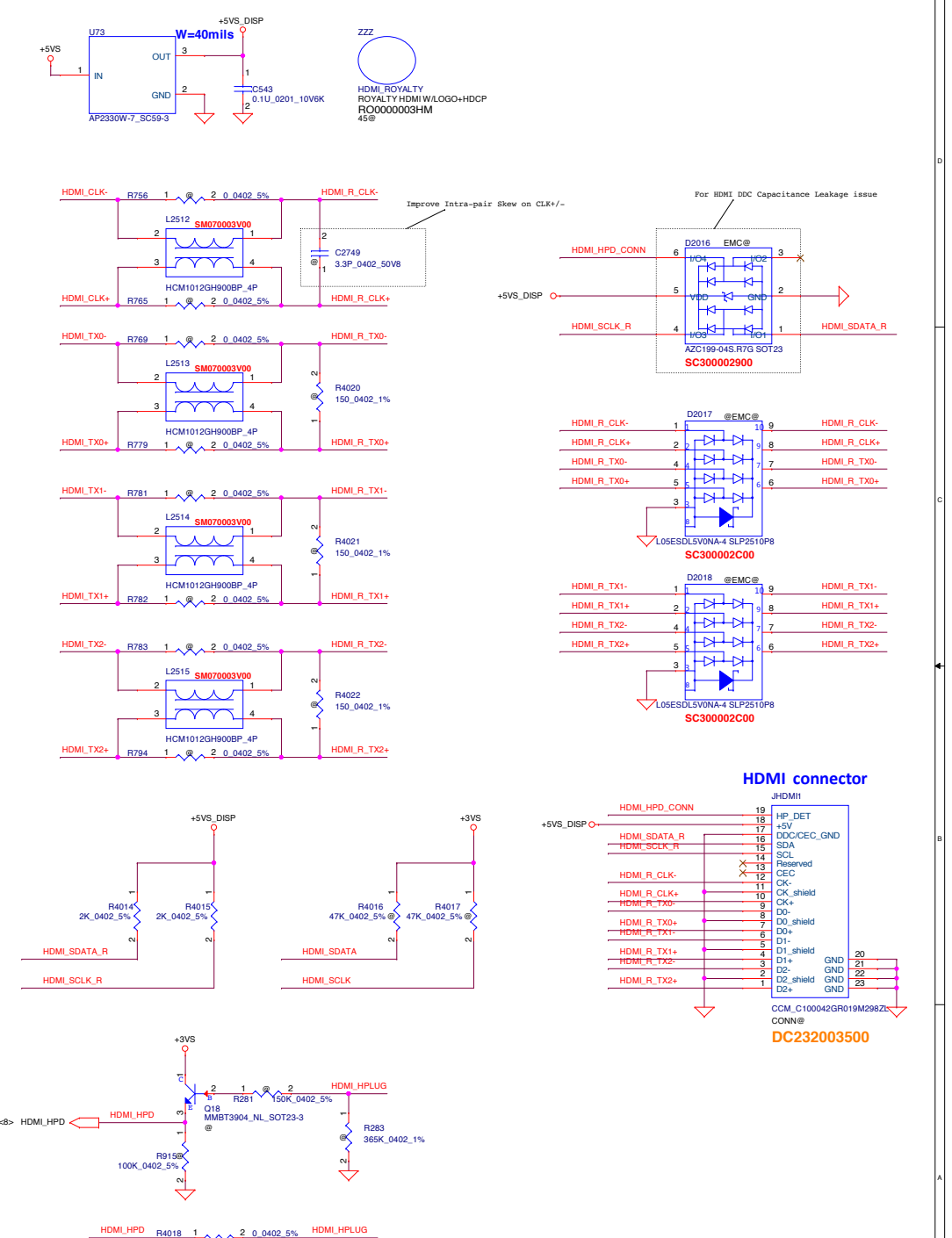
+1.8VALW TO +1.8VSDGPU



+3VS TO +3VSDGPU



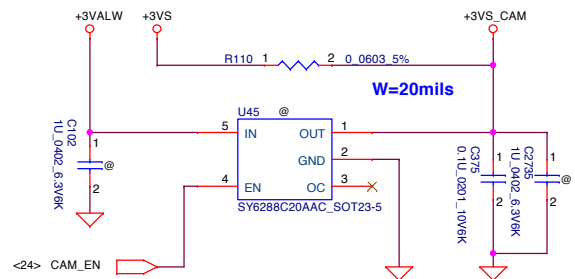
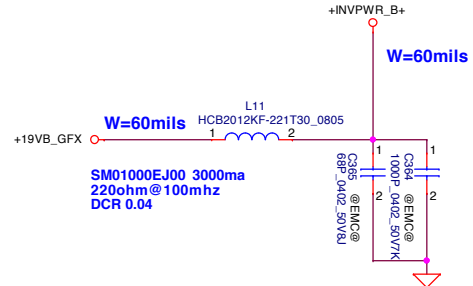
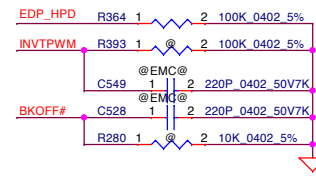
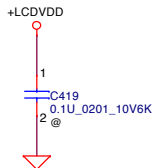
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						Size		Document		Rev	
						Custm		C5V08/D5PR8		LA-E903PR1A	
						Date:		Tuesday, May 02, 2017		Sheet 25 of 50	



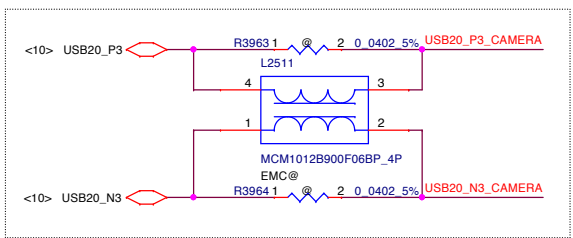
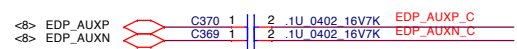
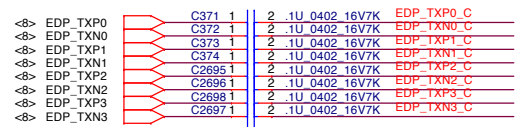
LCD POWER CIRCUIT

The diagram illustrates the LCD power circuit. It features a power supply section with a +3VS input and a 3V6V output. The LCD module (U8) is connected to this supply. The IN pin of U8 is connected to +3VS, and the OUT pin is connected to LCDVDD. The EN pin is connected to a 3V6V supply. A 0.1uF capacitor (C368) is connected between LCDVDD and ground. A 4.7uF capacitor (C367) is connected between LCDVDD and ground. The circuit is labeled with 'W=60mils' and 'C367 4.7U_0402_6.3V6M'.

A schematic diagram showing a capacitor labeled C419 with a value of 0.1uF 0201 10V6K. The capacitor is connected between a red node labeled +LCDVDD and a ground symbol (a red triangle pointing down). The capacitor is represented by two parallel blue lines. The text '1' is next to the top wire and '2' is next to the bottom wire, with a '@' symbol below the value.



<24> CAM_



5

W=60mils

JEDP1

ACES_50398-04041-001
CONN@

SP010013I00

D2015
@EMC@
YSLC05CH_SOT23-3

+INVTPWR_B+

INVT PWM
BKOFF#
EDP_HPD

EDP_AUXN_C
EDP_AUXP_C
EDP_TXP0_C
EDP_TXN0_C
EDP_TXP1_C
EDP_TXN1_C
EDP_TXP2_C
EDP_TXN2_C
EDP_TXP3_C
EDP_TXN3_C

+3VS_CAM
USB20_N3_CAMERA
USB20_P3_CAMERA

DMIC_CLK_R
DMIC_DATA

LCDVDD

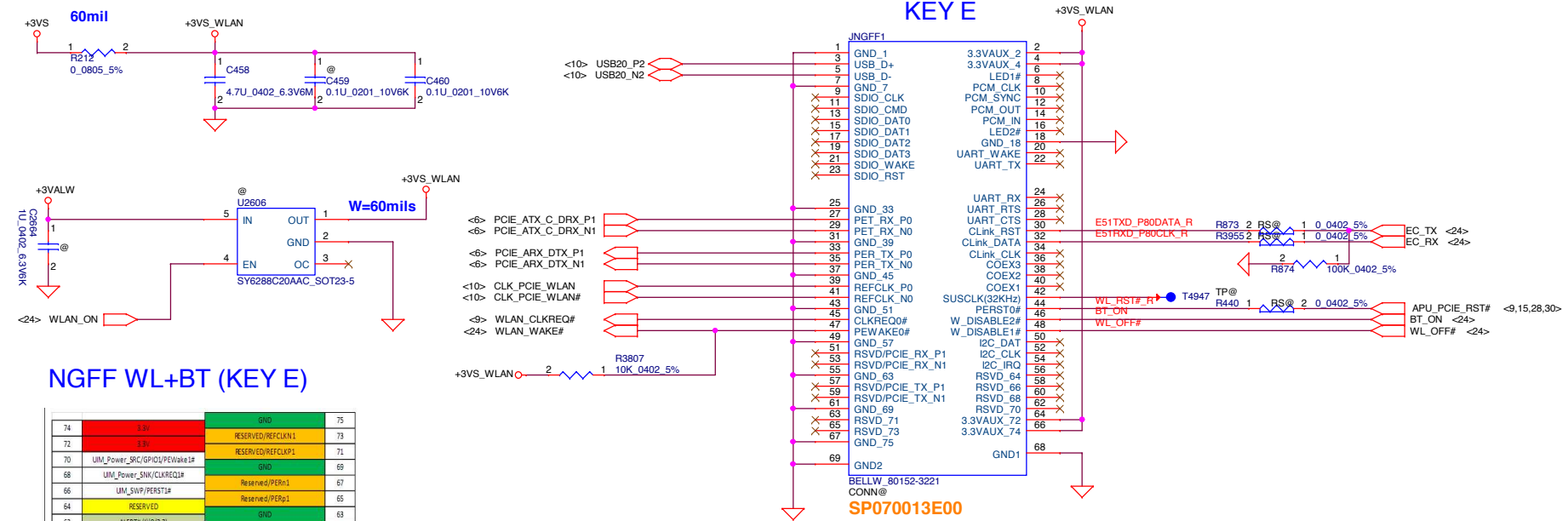
DMIC_CLK_R
DMIC_DATA

G1
G2
G3
G4
G5

--	--

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				Document Number C5V08/D5PR8_LA-E903PR1A	1.A
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Wireless LAN

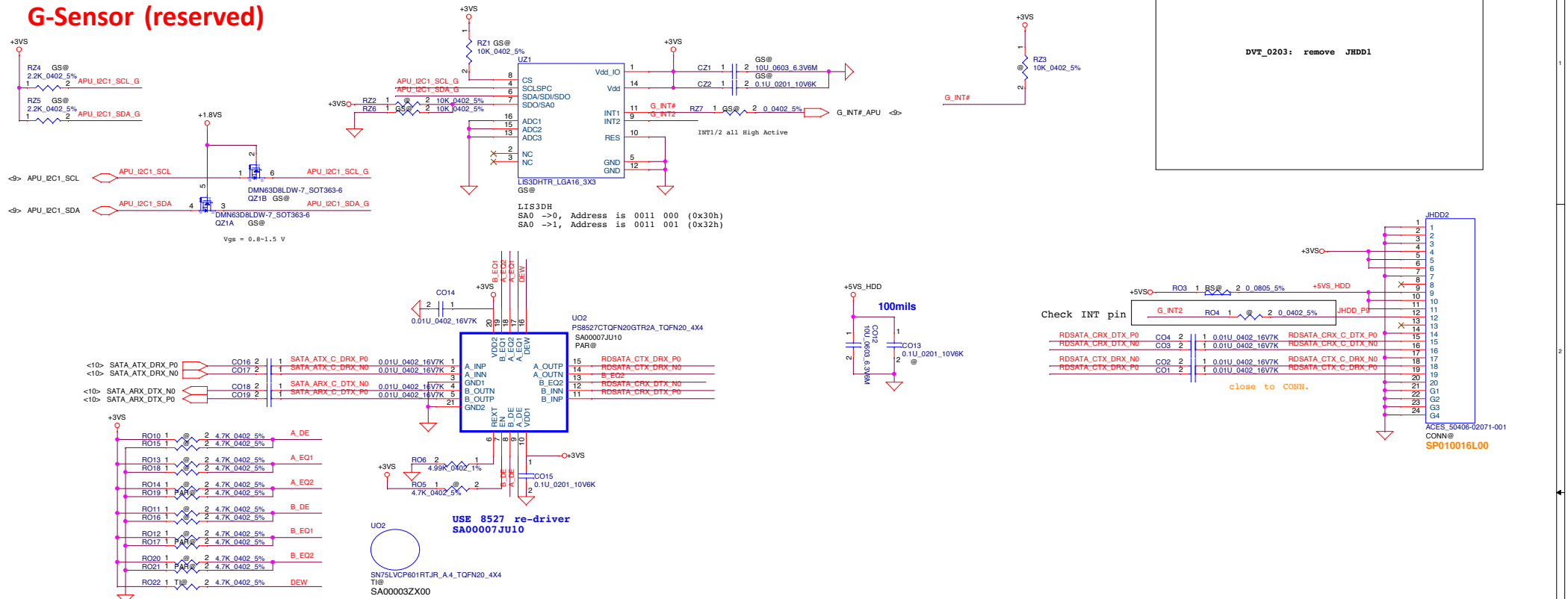


NGFF WL+BT (KEY E)

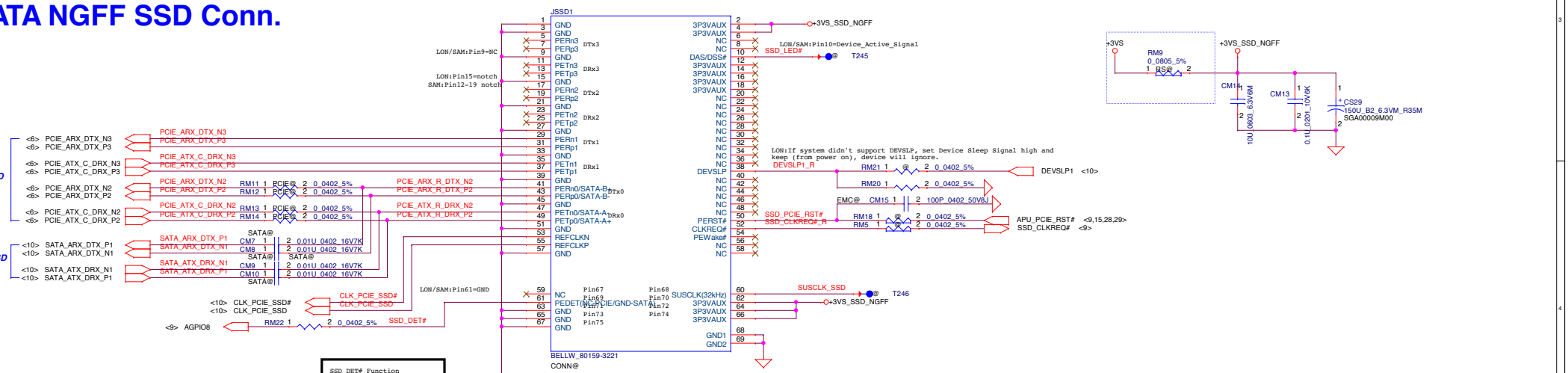
74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKN1	73
70	UIM_Power_SRC/GPIO/PEWake#	RESERVED/REFCLKP1	71
68	UIM_Power_SRC/CLKREQ1#	GND	69
66	UIM_SW/PERST#	Reserved/PERn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERT# (I/O)(3.3)	GND	63
60	DC CLK (I/O)(3.3)	Reserved/PETn1	61
58	DC DATA (I/O)(3.3)	Reserved/PETp1	59
56	W_DISABLE# (O)(0.3V)	GND	57
54	Reserved/W_DISABLE#2 (O)(0.3V)	REWake# (O)(0.3V)	55
52	PERST# (O)(0.3V)	CLKREQ# (O)(0.3V)	53
50	SUSCLK(32KHz) (O)(0.3V)	GND	51
48	COEX1 (I/O)(0.1.8V)	REFCLKP0	47
46	COEX3 (I/O)(0.1.8V)	GND	45
44	COEX3 (I/O)(0.1.8V)	PERn0	43
42	VENDOR DEFINED	PERp0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PETn0	37
36	UART RTS (I/O)(1.8V)	PETp0	35
34	UART CTS (I/O)(1.8V)	GND	33
32	UART Tx (O)(0.1.8V)	RESERVED/REFCLKN1	31
30	RESERVED/REFCLKP1	RESERVED/REFCLKN1	29
28	RESERVED/REFCLKP1	RESERVED/REFCLKN1	27
26	RESERVED/REFCLKP1	RESERVED/REFCLKN1	25
24	RESERVED/REFCLKP1	RESERVED/REFCLKN1	23
22	UART Rx (I/O)(1.8V)	SDIO Wake# (O)(0.1.8V)	21
20	UART Wake# (I/O)(3.3V)	SDIO DAT3 (O)(0.1.8V)	19
18	GND	SDIO DAT2 (O)(0.1.8V)	17
16	LED#1 (I/O)	SDIO DAT1 (O)(0.1.8V)	15
14	PCM_OUT/DS_SD_OUT (O)(0.1.8V)	SDIO DAT0 (O)(0.1.8V)	13
12	PCM_IN/DS_SD_IN (I/O)(1.8V)	SDIO CMD (O)(0.1.8V)	11
10	PCM_SYNC/DS_WS (O)(0.1.8V)	SDIO CLK (O)(0.1.8V)	9
8	PCM_CLK/DS_SCK (O)(0.1.8V)	GND	7
6	LED#1 (I/O)	LED#1 (I/O)	5
4	3.3V	USB_D+	3
2	3.3V	GND	1

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Size	Custom	Document Number	C5V08/D5PR8_LA-E903PR1A	Rev	1.A
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SATA Re-Driver and cable HDD Conn.

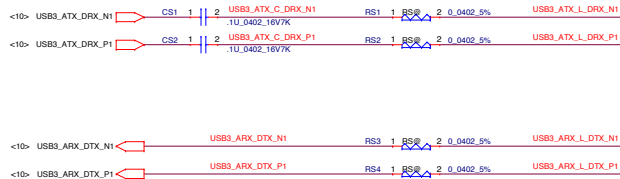


SATA NGFF SSD Conn.



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USB3.0 (Port 1)



USB3.0 (Port 2)

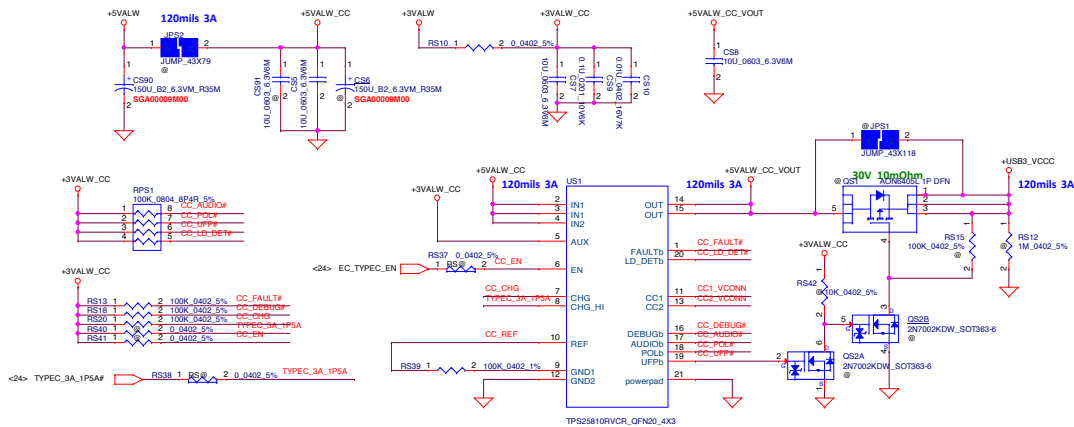
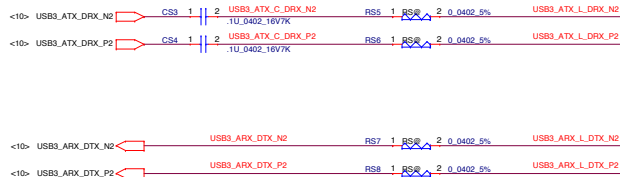


Table 3. USB Type-C Current Advertisement

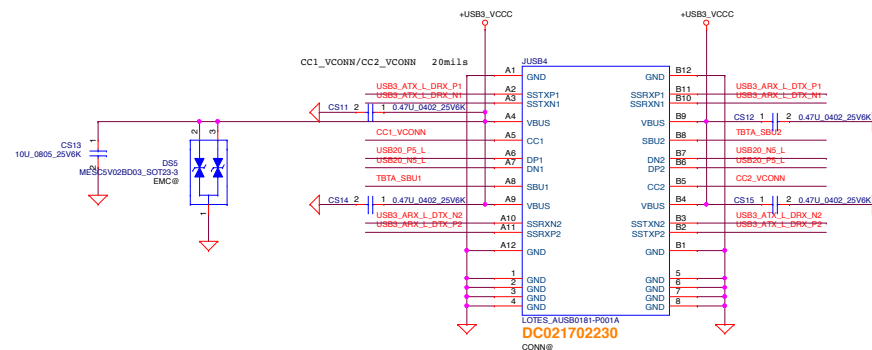
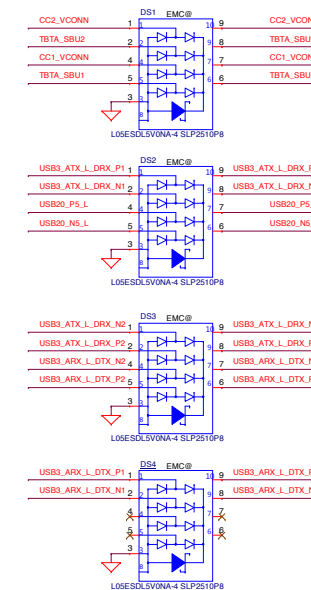
CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

EC_TYPEC_EN	S0	S3	S5
AC Mode (Adapter In)	On	On	Off
DC Mode (Battery Only)	On	On ¹	Off

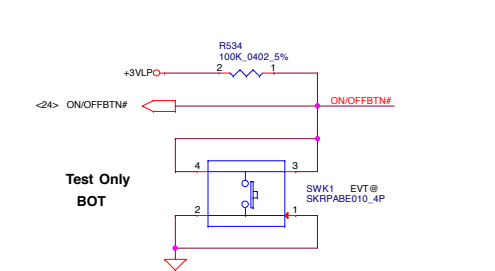
Note 1: Stop charge current when the battery capacity is below a specified percentage.

Note : 2017 BIOS SPEC define DC mode 30% stop charge

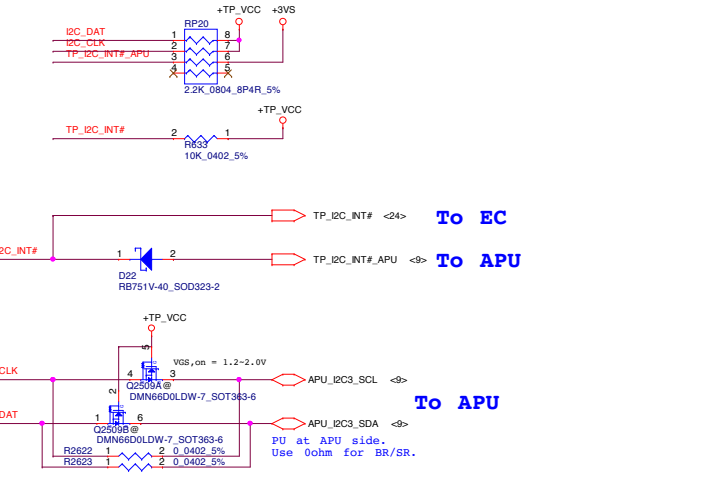
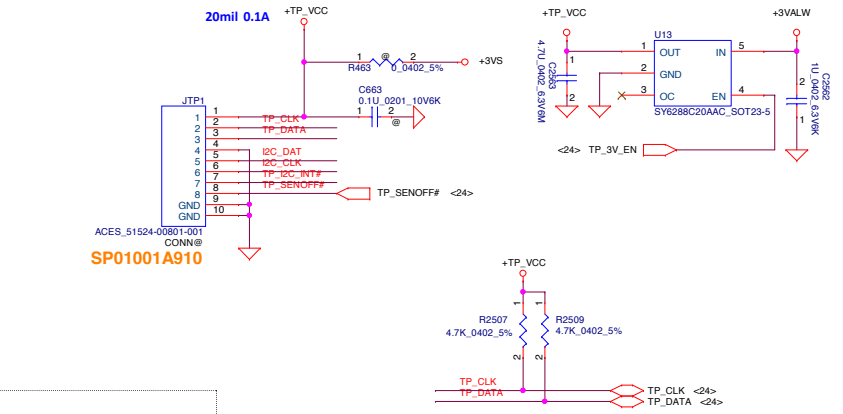
For ESD request



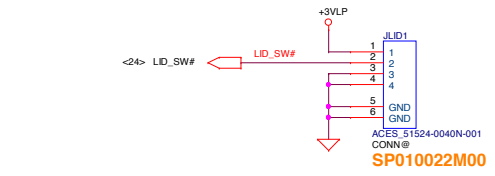
ON/OFF BTN



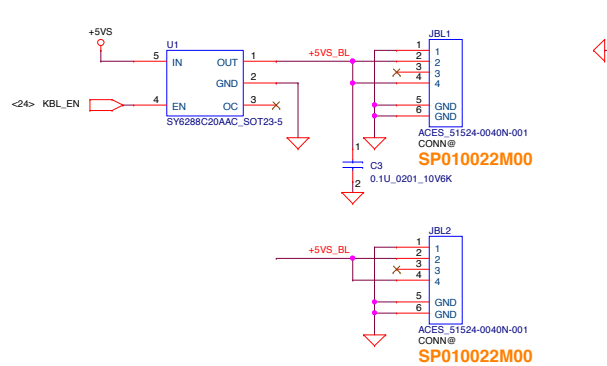
TP/B Conn.



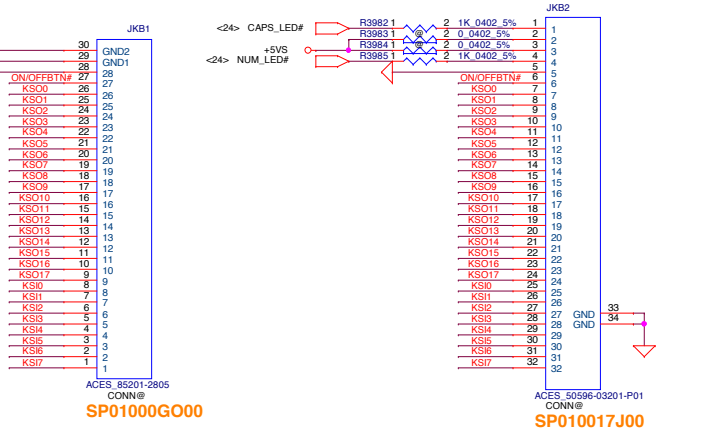
Lid Switch (Hall Effect Switch)



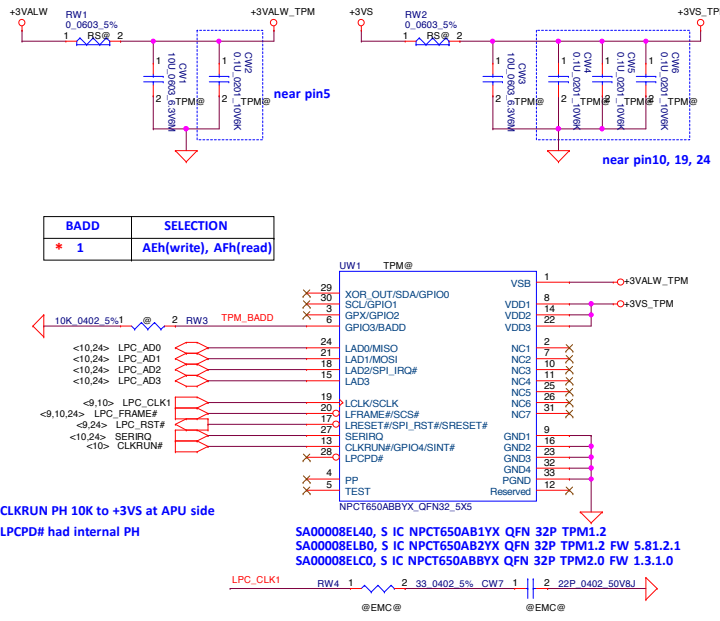
KB BackLight



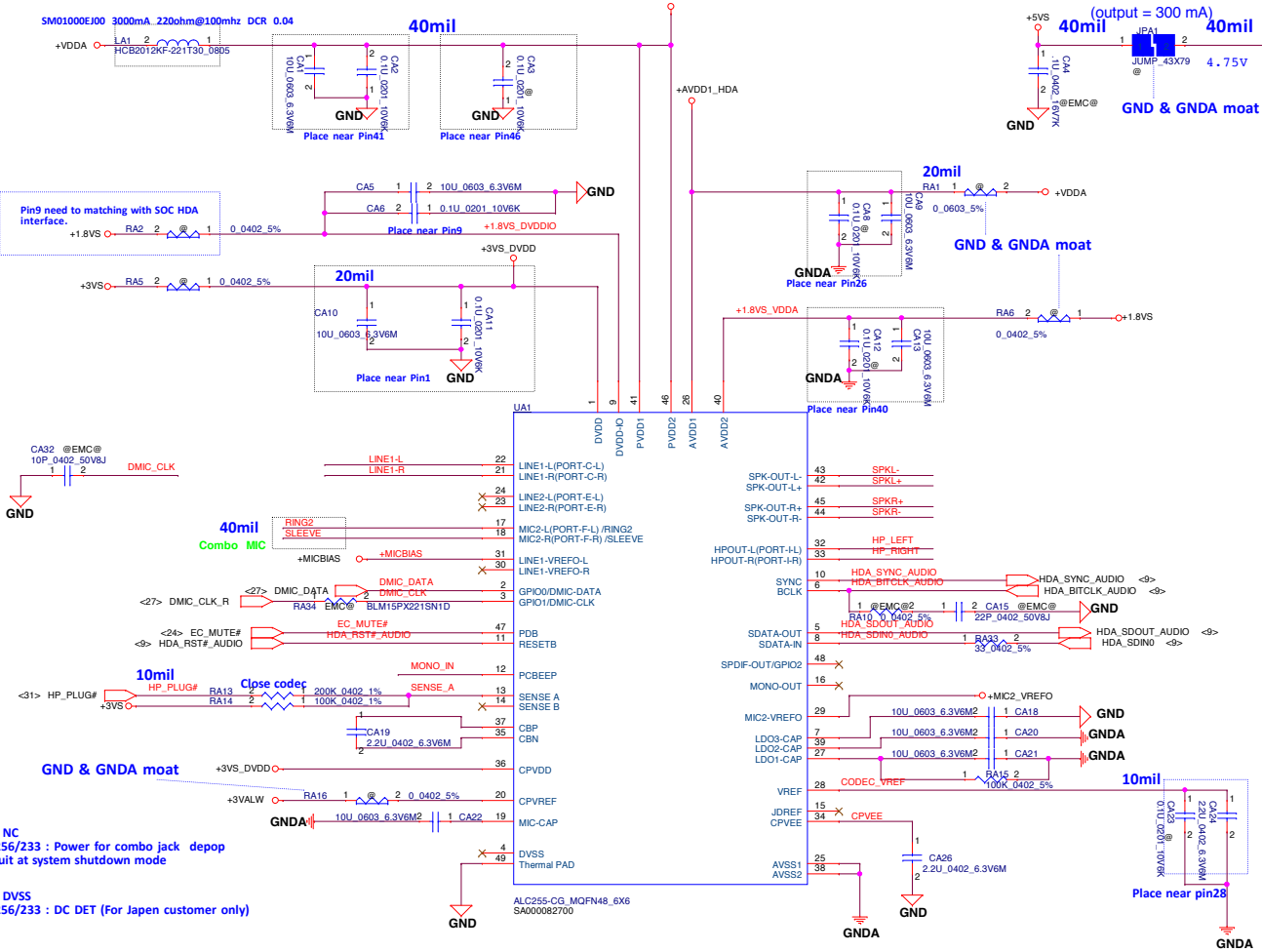
KB Conn.



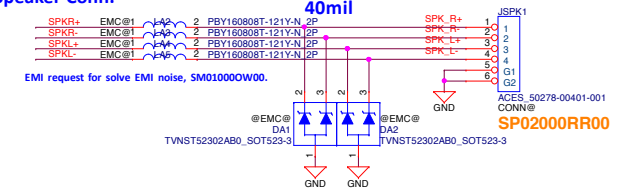
TPM



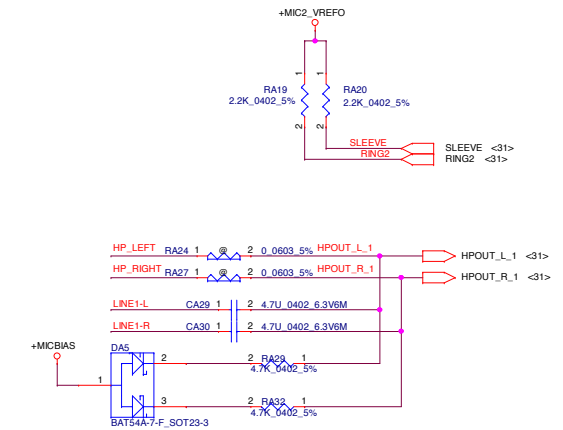
HD Audio Codec



Int. Speaker Conn.

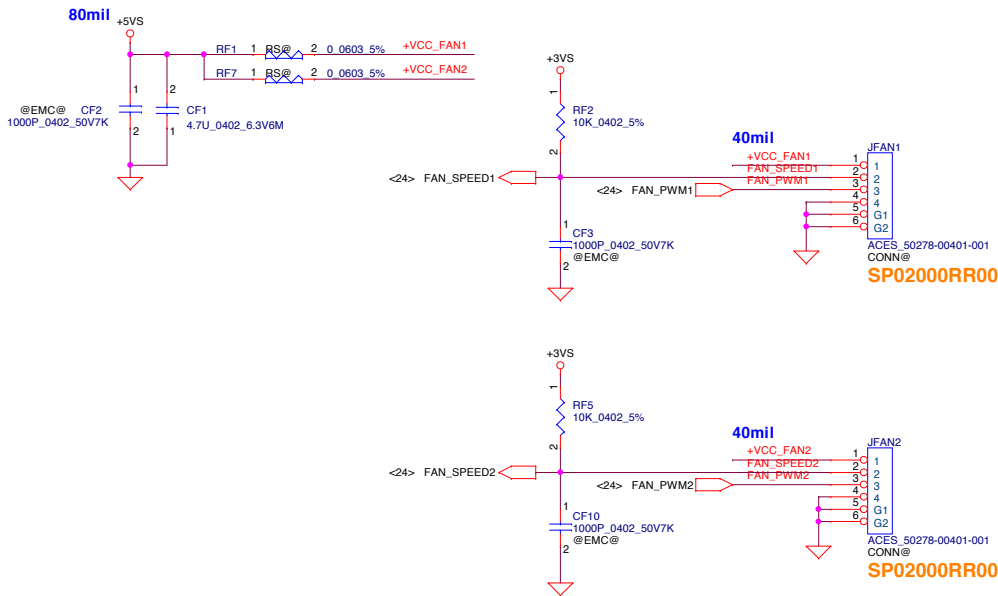


Headphone Out

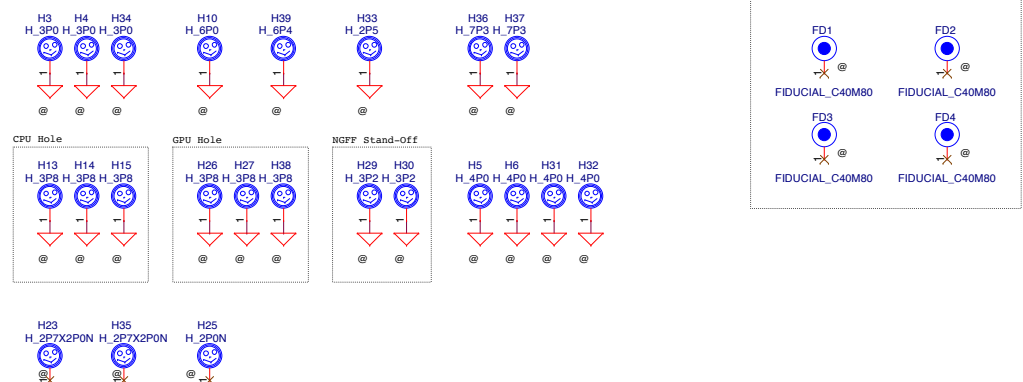


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				Customer	C5V08/D5PR8_LA-E903PR1A
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				Sheet	34 of 50

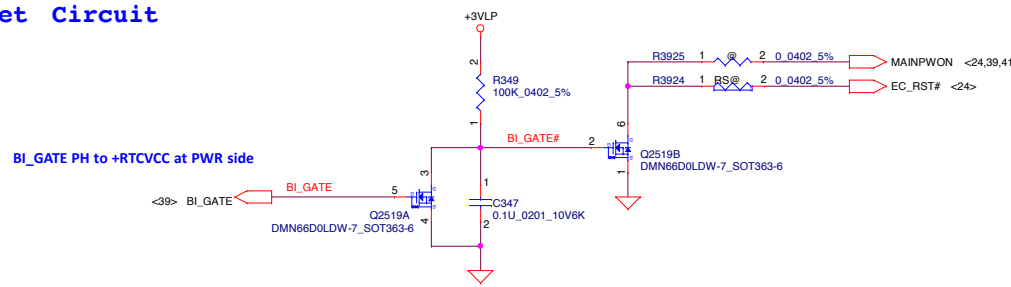
FAN Conn



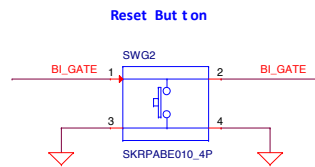
Screw Hole



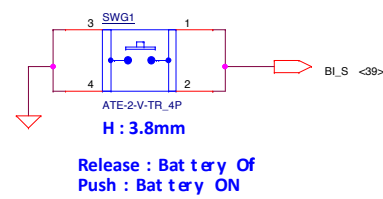
Reset Circuit



Reset But t on



BI SW



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								C5V08/D5PR8_LA-E903PR1A	
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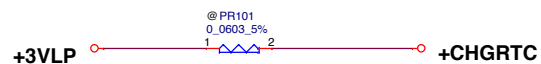
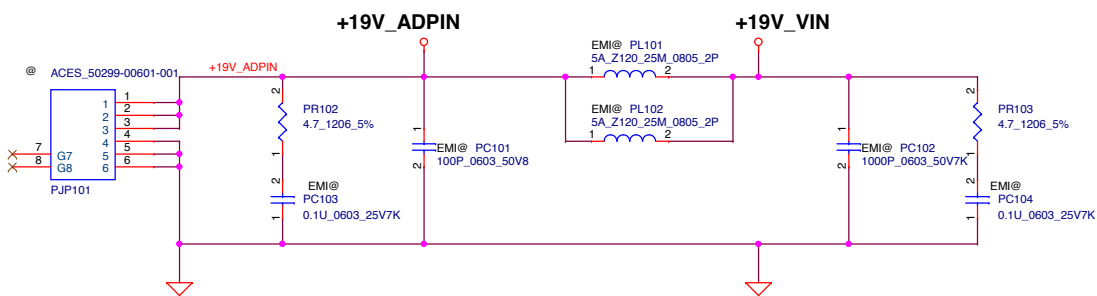
		5	Version Change List (P. I. R. List)		3	Page 1		2			1																																		
Item	Page#	Date	Request Owner	Issue Description	Solution Description	Rev.																																							
D	1	02/03		1. update SR PN 2. update VRAM strap (add MICRON) 3. R4000 --> @, R3999 --> RX560@, add R4002 for UMA@ 4. QZ1 change to SB000013K00 5. H29,H30 change to H_3P2 6. CD11,CD12,CD13,CD14,CD15,CD24,CD27,CD28,R3979 change to VX@ 7. change D103 to SC600000B00,add R4003 8. remove JHDD1 9. JPA8 change to JPS2 10.Q84,Q91,Q2511,QL1 change to SB00000PU10		1.0																																							
	2	02/22		1. Sync QL1 Symbol to Q84,Q91,Q2511 2. change SB00000PU10 to SB00000PU00 3. remove R4002 with UMA@, change R4002 to RX540@ 4. add CV2722 and unpop at VGA_ON_B 5. update UV56 PCB Footprint to from SOP8207mil to SOP8-150mil 6. RO19 change to pop 7. CS25 change to B2 footprint (SGA00009M00) 8. Q91,R1563 change to pop 9. R1562 pop with 100k,R1564 pop with 12k for DVT Board ID 10.RV440,RV422 change to @, RV423,RV439 change to DIS@ (VBIOS in SBIOS) 11.Combine 02/22 Power 12.C794,C795 change to 4.7pF (SE07147AC80) 13.CL18,CL19 change to 15pF (SE071150J80),RL14 change to 1k (SD028100180)		1.0																																							
C	3	02/23		1. Change to 0-ohm Short : RV1632,RO3,RM9,R3924,R683,RD8,RD9,RD10,RD246,RD252,RD225,RD250,RV1640,RS37,RS38 2. RS20 change with 100k 3. RA34 change with bead (SM01000NY00)		1.0																																							
	4	02/24		1. CLRP1 change to 0603 footprint 2. UV56 change to @ 3. RV1632 change to 0-ohm 4. Add R106 EMC@ 5. Combine Power 02/24		1.0																																							
B	5	03/01		1. 0-ohm short:R106,R107,R108,R3963,R3964,RS1,RS2,RS3,RS4,RS5,RS6,RS7,RS8 2. CV2723 add to @ 3. update JUSB4 Symbol (DC021702230) 4. L2509,L2510 add to EMC@		1.0																																							
	6	03/03		1. CS90 add to pop, CS91 add to @, CS6 change to @ 2. combine power 0303		1.0																																							
A	7	03/06		1. C2735 add to @		1.0																																							
	8	03/07		1. R4002 add to UMA@ 2. RO17,RO21 pop with PAR@ 3. R1564 add to VX@ with 27k (SD034270280) 4. update board ID table for VX 5. update UV1 PN, add DAZ PN		1.0																																							
	9	03/08		1. CD20,CD84 change to VX@ 2. CM15 pop with 100pF (SE071101J80) 3. RM22 change to VX@		1.0																																							
	9	03/09		1. RM22 change to pop		1.0																																							
	10	03/11		1. Add HDMI Redriver circuits (PS8409) 2. combine power 0310 3. L11 change to pop (remove NON2S@)		1.0																																							
	11	03/13		1. add 35W APU PN 2. U2615 change to SA0000AC310 3. update PCB PN,DAZ PN 4. C2748 add to pop		1.0																																							
				<table><tr><td>Security Classification</td><td colspan="3">Compal Secret Data</td><td colspan="3">Compal Electronics, Inc.</td></tr><tr><td>Issued Date</td><td>2017/04/18</td><td>Deciphered Date</td><td>2019/04/18</td><td colspan="3">Title</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td>Size</td><td>Document Number</td><td>Rev</td></tr><tr><td colspan="4"></td><td>Custom</td><td>C5V08/D5PR8_LA-E903PR1A</td><td>1.A</td></tr><tr><td colspan="4"></td><td>Date:</td><td>Tuesday, May 02, 2017</td><td>Sheet 36 of 50</td></tr></table>							Security Classification	Compal Secret Data			Compal Electronics, Inc.			Issued Date	2017/04/18	Deciphered Date	2019/04/18	Title			THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev					Custom	C5V08/D5PR8_LA-E903PR1A	1.A					Date:	Tuesday, May 02, 2017	Sheet 36 of 50
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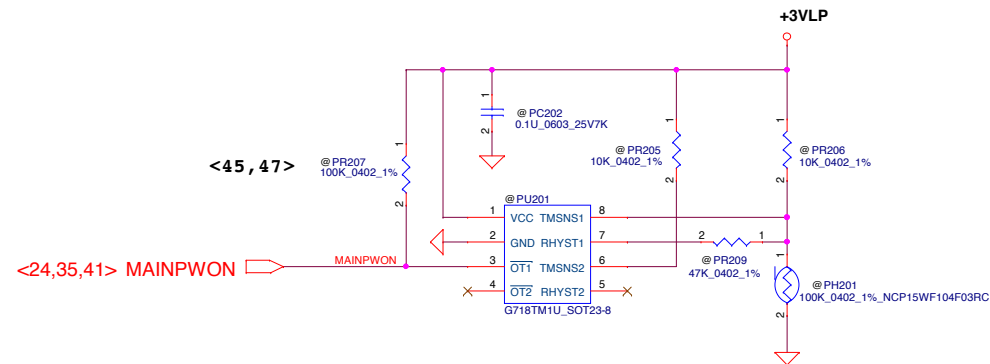
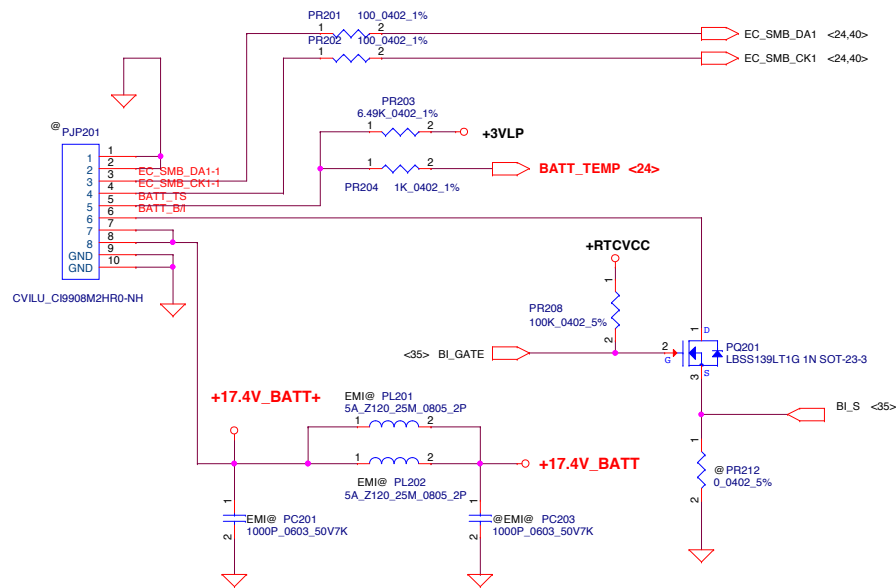
Item	Page #	Date	Request Owner	Issue Description	Solution Description	Rev.
12		03/17		1. R3979,CD11,CD12,CD13,CD14,CD15,CD27,CD28,CD24,CD20,CD84	change to pop without VX@.	1.0
13		04/10		1. U4 change main source to S TR A04354 1N SOIC-8 (SB000000ZN00) 2. Combine power schematic with 0407		1.A
14		04/11		1. L2512,L2513,L2514,L2515	add to pop with 90-ohm choke (SM070003V00)	1.A
15		04/18		1. R1564 change to 15k_0402_1% (SD034150280) for EA, 33K_0402_1% (SD034330280) for Vx 2. PCB change to Rev1A (DAZ21800201) 3. R4007 change to pop		1.A

1.A

1.A



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Size	Custom	Document Number	C5V08/D5PR8_LA-E903PR10	Rev	1.0
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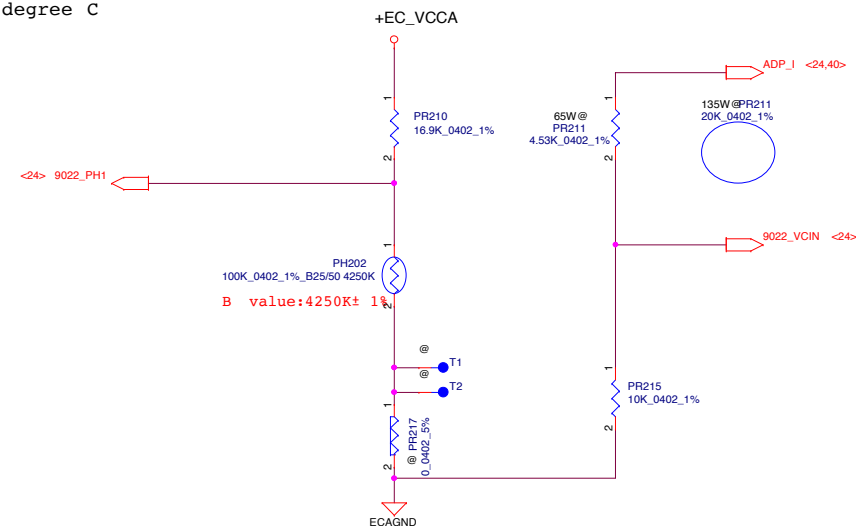
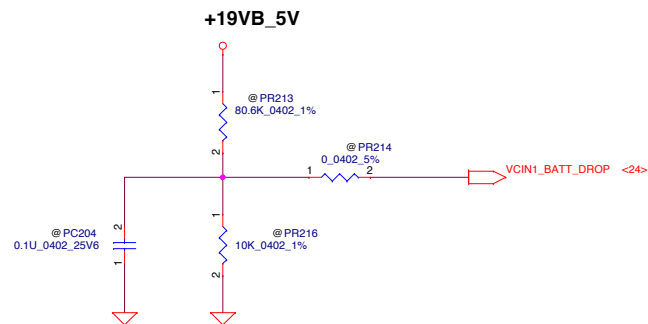
For KB9022 OTP	Active	Recovery
VCIN0_PH (V)	92C, 1V	56C, 2.V
PH202 (ohm)	7.3092K	26.11K

For KB9012 sense 20mΩ	Active	Recovery
SR 45W	58.5W, 0.61V	58.5W, 0.61V
BR 65W	84.5W, 0.61V	84.5W, 0.61V

PH202 under CPU bottom side :
 CPU thermal protection at 96 degree C (shutdown)
 Recovery at 56 degree C

2013/10/02
 Add for ENE9022 Battery Voltage drop detection.
 Connect to ENE9022 pin64 AD1.

Reserve for 2-cell design



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						Size	Document	Number	Rev	
						Custm	C5V08/D5PR8_LA-E903PR10			1.0
						Date:	Tuesday, May 02, 2017		Sheet	39 of 50

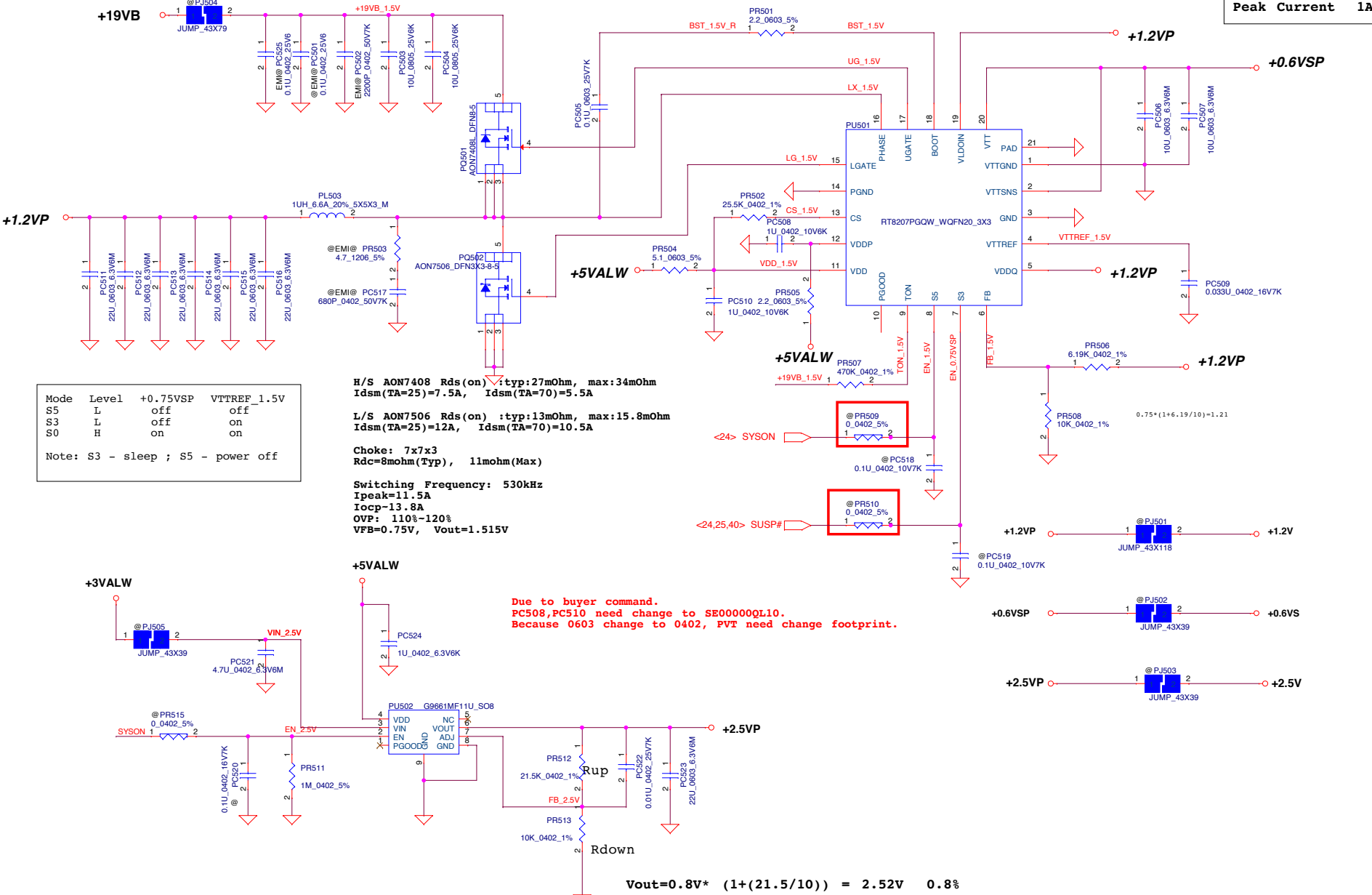
max Power loss 0.22W for 90W, Isat: 4A
(PR303 need change 10m ohm); DCR: 27mohm
0.12W for 65W system
CSR rating: 1W
VACP-VACN spec < 80.64mV

ID= 10.5A (Ta=70C)

1000

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

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				Size	Document Number	Rev
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Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

H/S AON7408 Rds(on):typ:27mOhm, max:34mOhm
Idsm(TA=25)=7.5A, Idsm(TA=70)=5.5A

L/S AON7506 Rds(on):typ:13mOhm, max:15.8mOhm
Idsm(TA=25)=12A, Idsm(TA=70)=10.5A

Choke: 7x7x3
Rdc=8mohm(Typ), 11mohm(Max)

Switching Frequency: 530kHz
Ipeak=11.5A
Iocp=13.8A
OVP: 110%-120%
VFB=0.75V, Vout=1.515V

Due to buyer command.
PC508,PC510 need change to SE00000QL10.
Because 0603 change to 0402, PVT need change footprint.

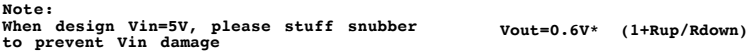
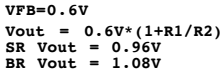
$$V_{out} = 0.8V * (1 + (21.5/10)) = 2.52V \quad 0.8\%$$

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

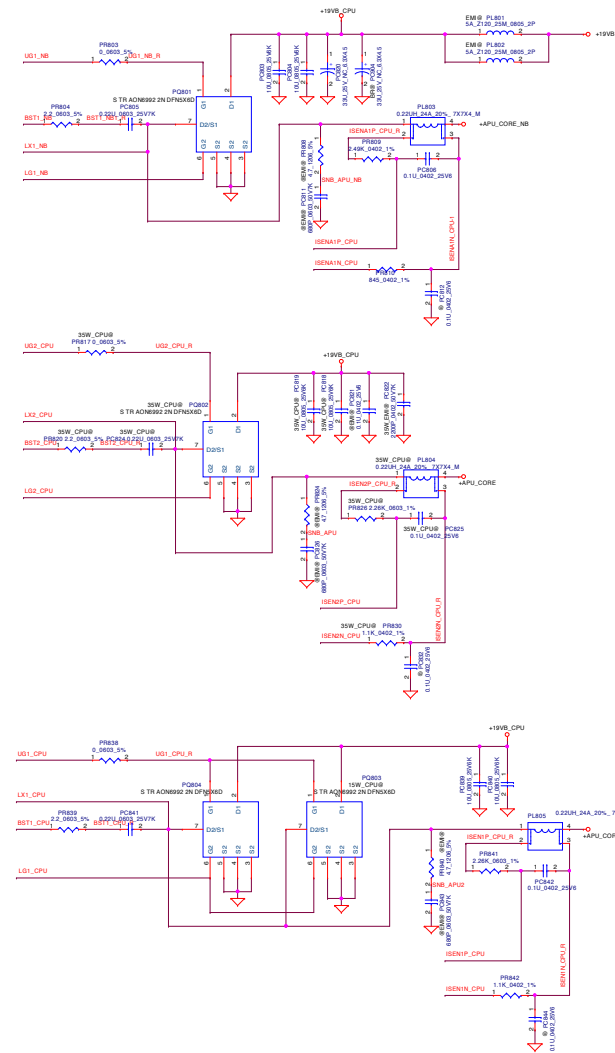
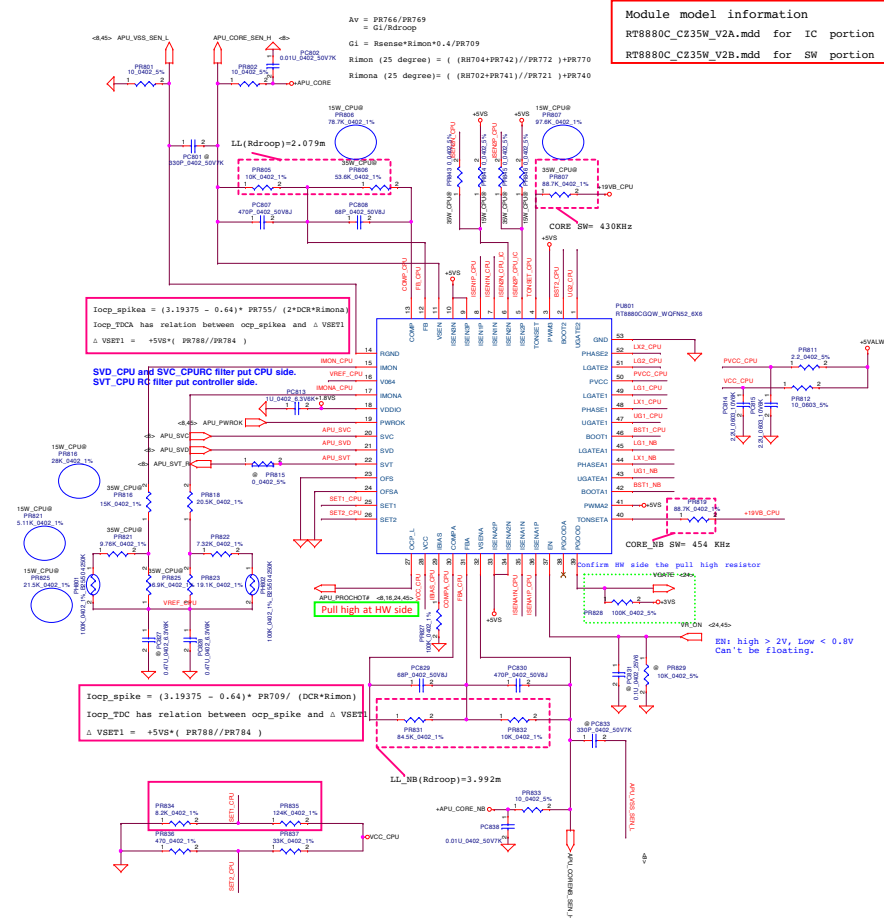
0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A

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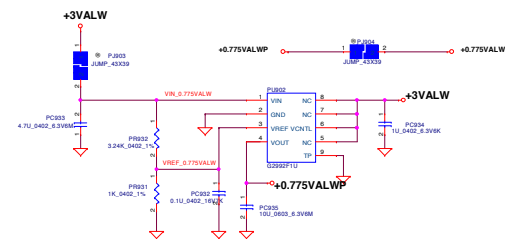

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Module model information
SY8208D_V1.mdd
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				Rev	1.0
				Page	1 of 1



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				RT888CGQW
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				Issue Date
				Date Issued: Mar 22 2017 Sheet 43 of 50

+APU_CORE

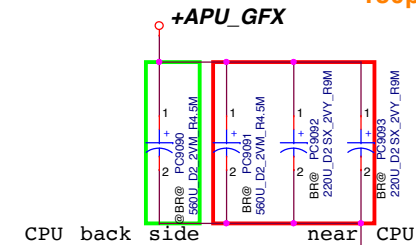
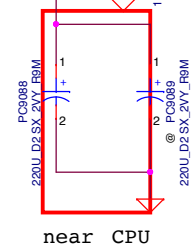
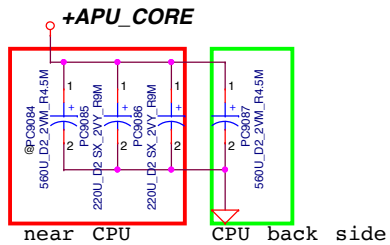
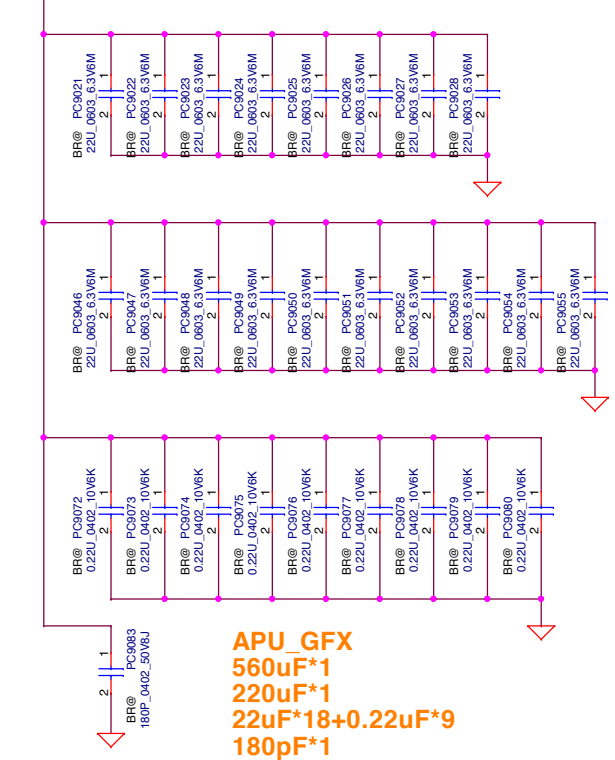
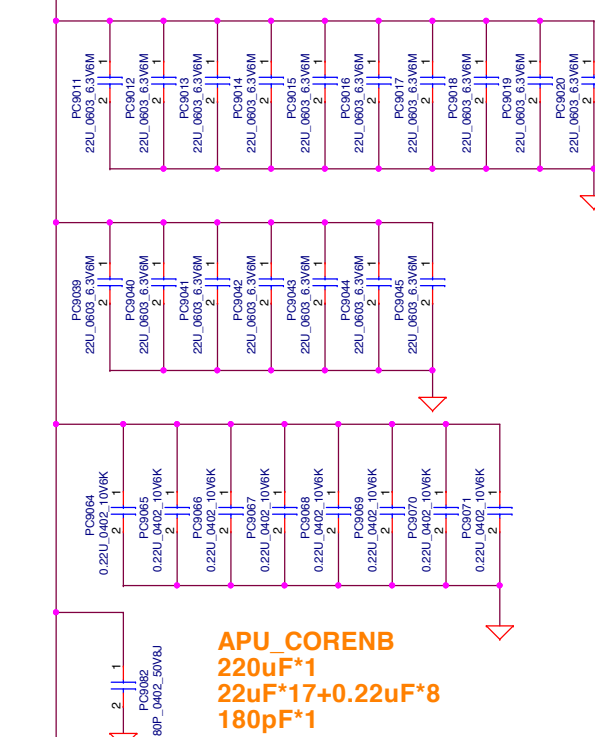
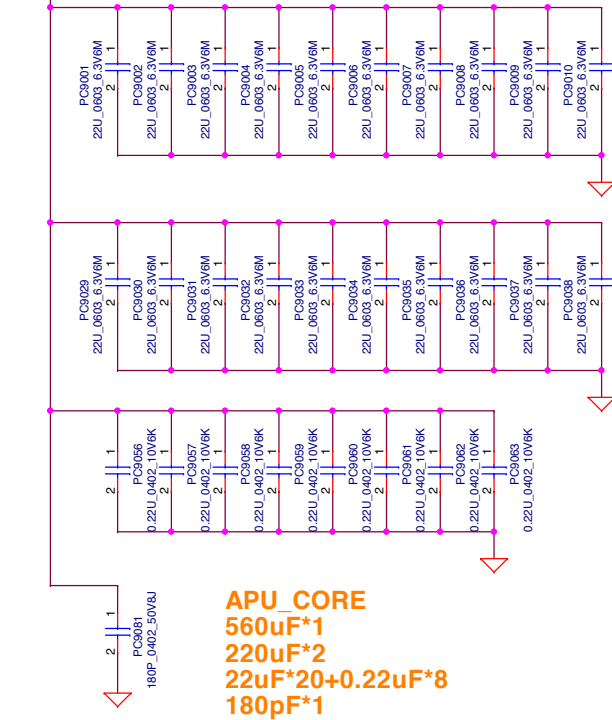
+APU_CORE_NB

+APU_GFX

+APU_CORE

+APU_CORE_NB

+APU_GFX

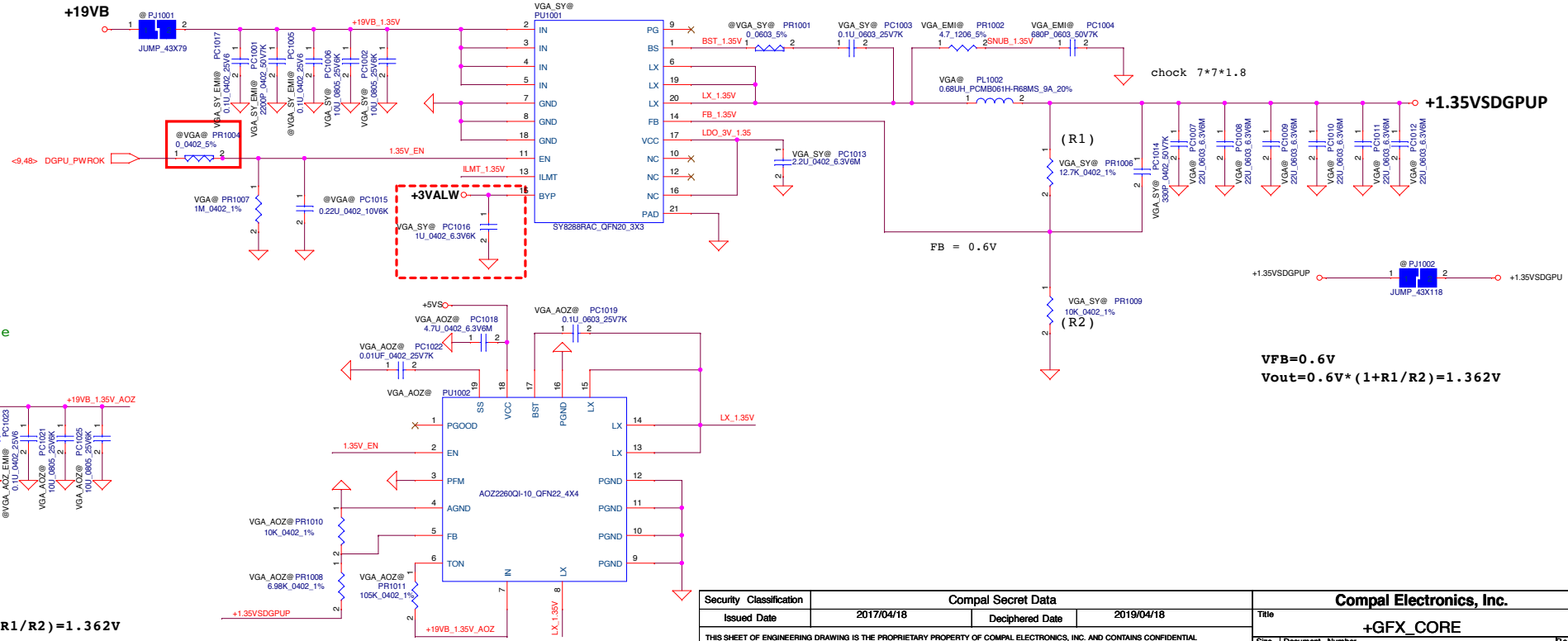


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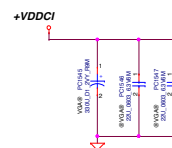
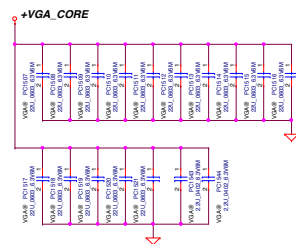
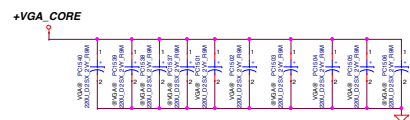
EA (C5V08): POP VGA_SY
VX (D5PR8): POP VGA_AOZ

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

Module model information
SY8208D_V1.mdd



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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	for EMI request	for EMI request	02	28 29 30 33	pop PL301, PL403, PL501, PL901, PL902		
02	VSEN_GFX duplicate net name	VSEN_GFX duplicate net name		01	PC1418 net name VSEN_GFX change to VSEN_VGA	2016/11/7	
03	SPOK_5V to EC	SPOK_5V to EC			PR410 change to 100K add SPOK_5V net	2016/11/17	
04	For B+ shape 變	APU_GFX input change to +19VB_APU from +19VB				2016/11/17	
05	FAE suggest	Add 3/5V input cap			add PC421, pc422	2016/12/1	
06	boost voltage is 12V	boost voltage is 12V			PR1603 change to 88.3K	2016/12/1	
07	HW request	HW request			delete PC923, PR926,PC927, PR929,PC930	2016/12/1	
08	follow BQ24735 module	follow BQ24735 module			PC321 change to 2200P from 0.22u	2016/12/12	
09	機構限 高	CPU 限高 2 , 變 F 放外面			PC9084 , PC909 改上 5 6 0	2016/12/13	
10	HW command	PL1602 unpop			PL1602 unpop	2017/02/02	
11	Design change	VX: delete PQ803 and PQ903 PR405 change P/N. EA: delete PC1024, PC1406, PL1602 Add PC9087 PR405 change P/N.			VX: PR211 change to 49.9k from 19.1k delete PL1602 EA: delete PC1024, PC1406, PL1602	2017/02/20	
12	Add VDDCI output cap	Add VDDCI output cap			Add PC1545 220uF	2017/02/20	
13	VDDCI ripple not meet spec.	change VDDCI design			PL1402 change to 0.47uH from 0.22uH PR1414 change to 2.37k from 1.24k PR1408 change to 37.4k from 137k PC1545 change to 330uF from 220uF	2017/02/23	
14	Follow ABO MOS pool	Follow ABO MOS pool			PQ502 change to AON7506 from SI7716	2017/02/23	
15	Follow ME and Thermal command	PC1503, PC1537, PC1538, PC1539 change to unpop PC1505 change to pop			PC1503, PC1537, PC1538, PC1539 change to unpop PC1505 change to pop	2017/03/07	
16	Design change	PC9084 change to unpop			PC9084 change to unpop	2017/03/07	
17	Design change	PR304 change to 0.01 ohm(SD00000K820) from 0.02 ohm PC820, PC904 change to SF000007700 from SF000007200 135W: PR211 SD034200280, S RES 1/16W 20K +-1% 0402 65W: PR211 SD034453180, S RES 1/16W 4.53K +-1% 0402			PR304 change to 0.01 ohm(SD00000K820) from 0.02 ohm PC820, PC904 change to SF000007700 from SF000007200 135W: PR211 SD034200280, S RES 1/16W 20K +-1% 0402 65W: PR211 SD034453180, S RES 1/16W 4.53K +-1% 0402	2017/03/09	
18	Design change	Due to C5V08/D5PR8 no use 2 cell battery, boost circuit change to unpop			PR213, PR214, PR216, PC204 change to unpop Boost circuit change to unpop, total 19 parts	2017/03/10	
19	HW command	boost circuit change to delete			boost circuit change to delete	2017/03/10	
20	變 c o m m a n d	PC814, PC815, PC914, PC915 change to SE000003H00 from SE00000GC00			PC814, PC815, PC914, PC915 change to SE000003H00 from SE00000GC00	2017/03/14	
21	PVT change: 變 c o m m a n d	PC401,PC419,PC508,PC510,PC1465 change from SE080105K80 to SE00000QL10 PC1428,PC1429 change from SE135105K80 to SE00000OU00 PC506,PC507 change from SE093106K80 to SE000005T80 PC935 change from SE093106M80 to SE000005T80			PC401,PC419,PC508,PC510,PC1465 change from SE080105K80 to SE00000QL10 PC1428,PC1429 change from SE135105K80 to SE00000OU00 PC506,PC507 change from SE093106K80 to SE000005T80 PC935 change from SE093106M80 to SE000005T80	2017/03/21	
22	Design change	for delay adpi change PR324 from 0ohm to 499ohm change PQ201 from LBSS138 to LBSS139 for ESD protect			for delay adpi change PR324 from 0ohm to 499ohm change PQ201 from LBSS138 to LBSS139 for ESD protect		
23	Design change	change PR515, PR1452, PR1453, PR815, PR915, PR1410, PR1431, PR1424, PR1428 to R-short			change PR515, PR1452, PR1453, PR815, PR915, PR1410, PR1431, PR1424, PR1428 to R-short		

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